

NORBIT 2 TWIN INVERTER AMPLIFIER OR LOW POWER OUTPUT

2IA60

This data sheet should be read in conjunction with
NORBIT 2 Series

DESCRIPTION

The unit comprises two inverter amplifiers which may be interconnected to form either a single inverting low power output unit or a single non-inverting low power output unit.

COLOUR

Blue

ELECTRICAL DATA

Power supply

Supply voltage, V_P

$+24 \pm 25\%$ $V_{d.c.}$

Supply current to pin 16

max. 31 mA ←

Input

Logic '0'

0 to 0.3 V

Logic '1'

$+(0.24V_P + 7.2)$ to V_P V

Loading per input (all functions)

2 d.u.

Output

Loading per inverter amplifier output

20 d.u.

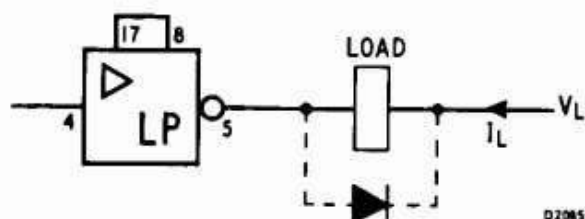
Loading, when used as load driver (see figs. 1 and 2)

Load voltage

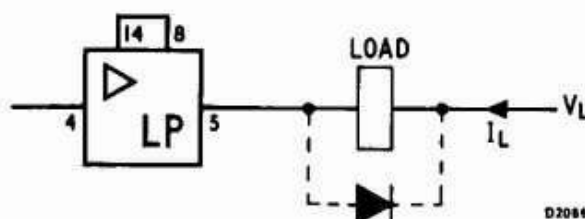
max. 30 V

Load current

max. 100 mA



Logic '1' at the input,
energises the load
Fig. 1



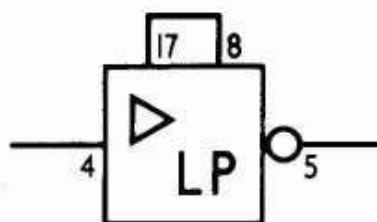
Logic '0' at the input,
energises the load
Fig. 2

NOTES

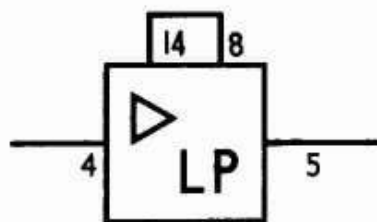
1. A diode must be used with inductive loads; suitable diodes are: BAX12, BAX13 or BAX16.
2. When driving filament lamps, series and bleed resistors must be used.

Mullard

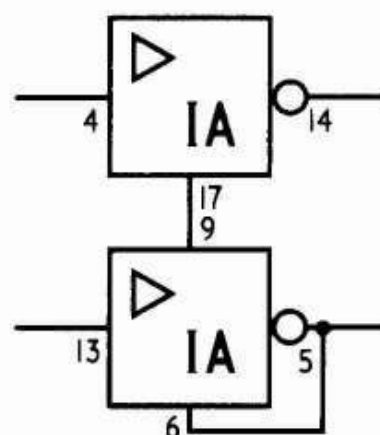
DRAWING SYMBOL



Inverting
low power output

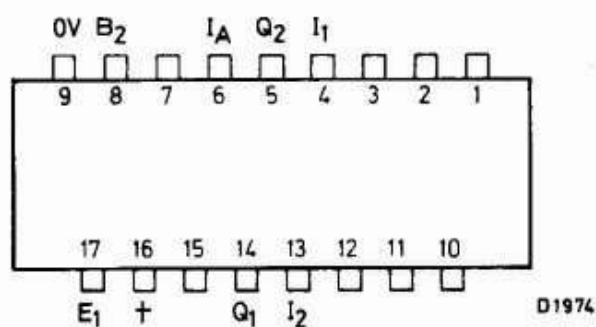


Non-inverting
low power output



2 × inverter
amplifier

TERMINAL CONNECTIONS



view from underside of module

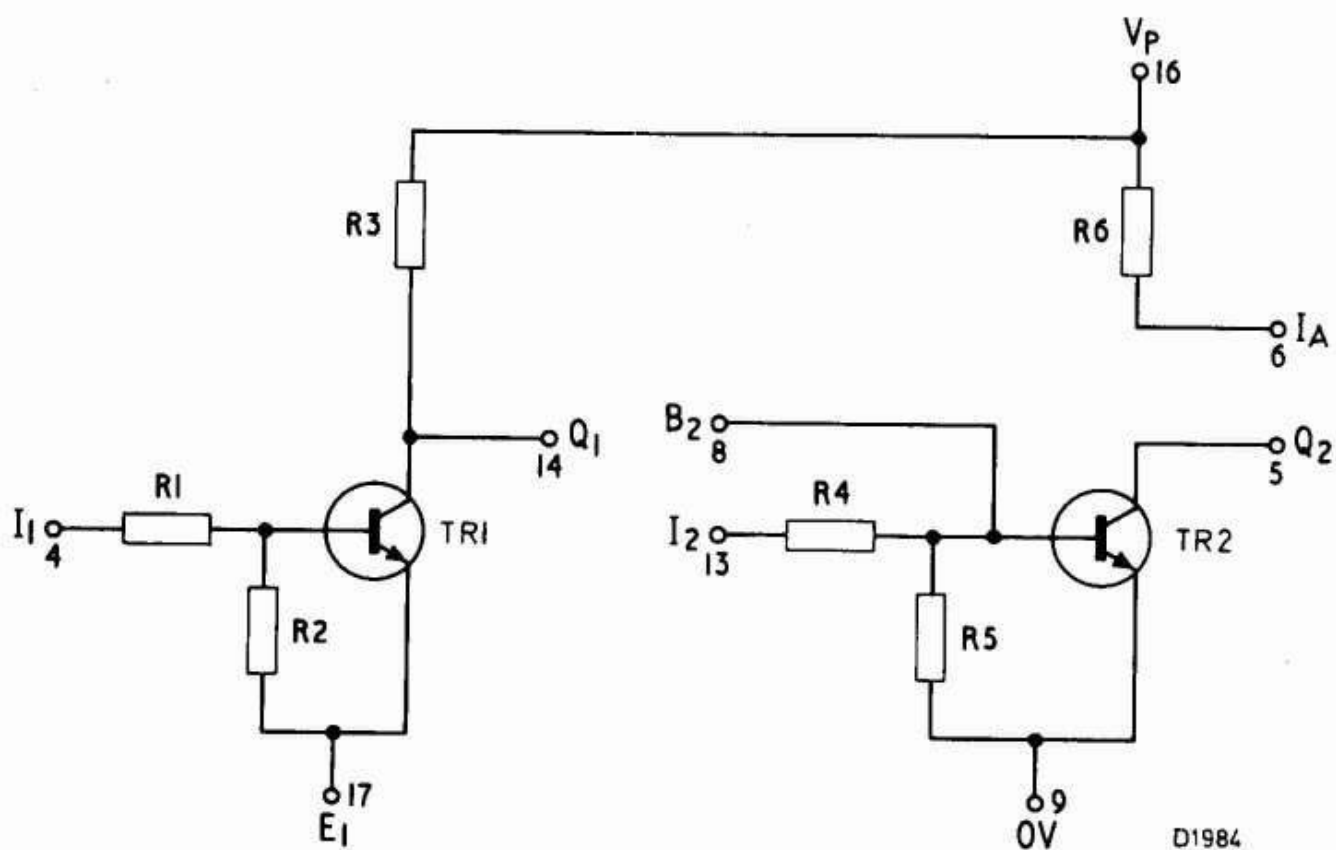
Terminal number	Connected to	Terminal number	Connected to
1	Not connected	10	Not connected
2	Not connected	11	Not connected
3	Not connected	12	Not connected
4	Input to IA 1 (I_1)	13	Input to IA 2 (I_2)
5	Output from IA 2 (Q_2)	14	Output from IA 1 (Q_1)
6	Collector resistor TR2 (I_A)	15	Not connected
7	Not connected*	16	Positive supply V_P (+)
8	Base of TR2 (B_2)	17	Emitter of TR1 (E_1)
9	Common supply (0V)		

*CAUTION When mounted on PCB60, pin 7 is connected to the positive supply (V_P). Hence, ensure that pins 7 and 8 are not interconnected otherwise damage to TR2 will result.

NORBIT 2 TWIN INVERTER AMPLIFIER OR LOW POWER OUTPUT

2IA60

CIRCUIT DIAGRAM



NORBIT 2 TWIN LOW POWER OUTPUT

2LPA60

This data sheet should be read in conjunction with
NORBIT 2 Series

DESCRIPTION

Two electrically independent inverting output driven circuits. The circuits are suitable for driving relays and small lamps.

COLOUR

Blue

ELECTRICAL DATA

Power supply

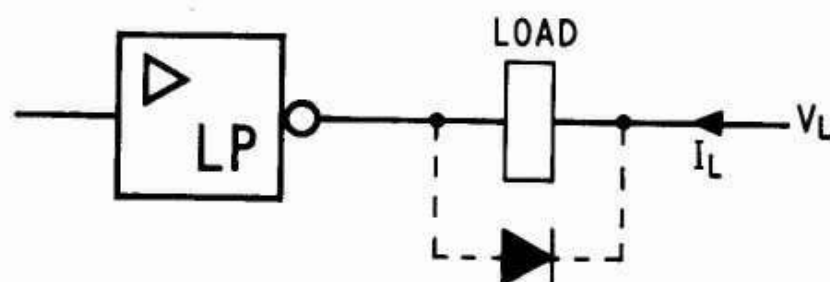
Supply voltage, V_P		$+24 \pm 25\%$	$V_{d.c.}$
Supply current to pin 7	max.	20	mA

Input

Logic '0'		0 to 0.3	V
Logic '1'		$+(0.24V_P + 7.2)$ to V_P	V
Loading per input		2	d.u.

Output (see fig. 1)

Load voltage	max.	30	V
Load current	max.	100	mA



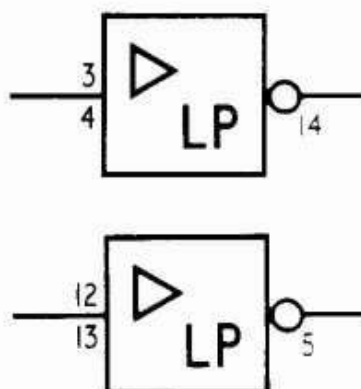
Logic '1' at the input
will energise the load
Fig. 1

NOTES

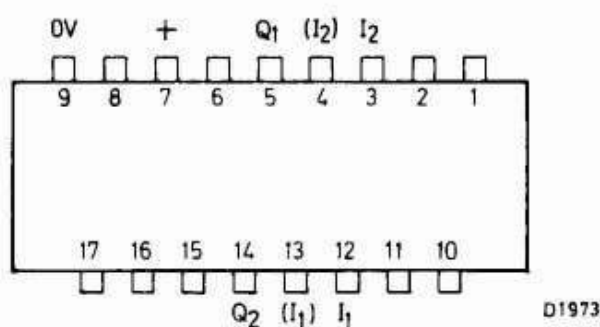
1. The load must be connected as shown to output pins 5 or 14 as required.
2. A diode must be used with inductive loads; suitable diodes are: BAX12, BAX13 or BAX16.
3. When driving filament lamps, series and bleed resistors must be used.

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DRAWING SYMBOL



TERMINAL CONNECTIONS



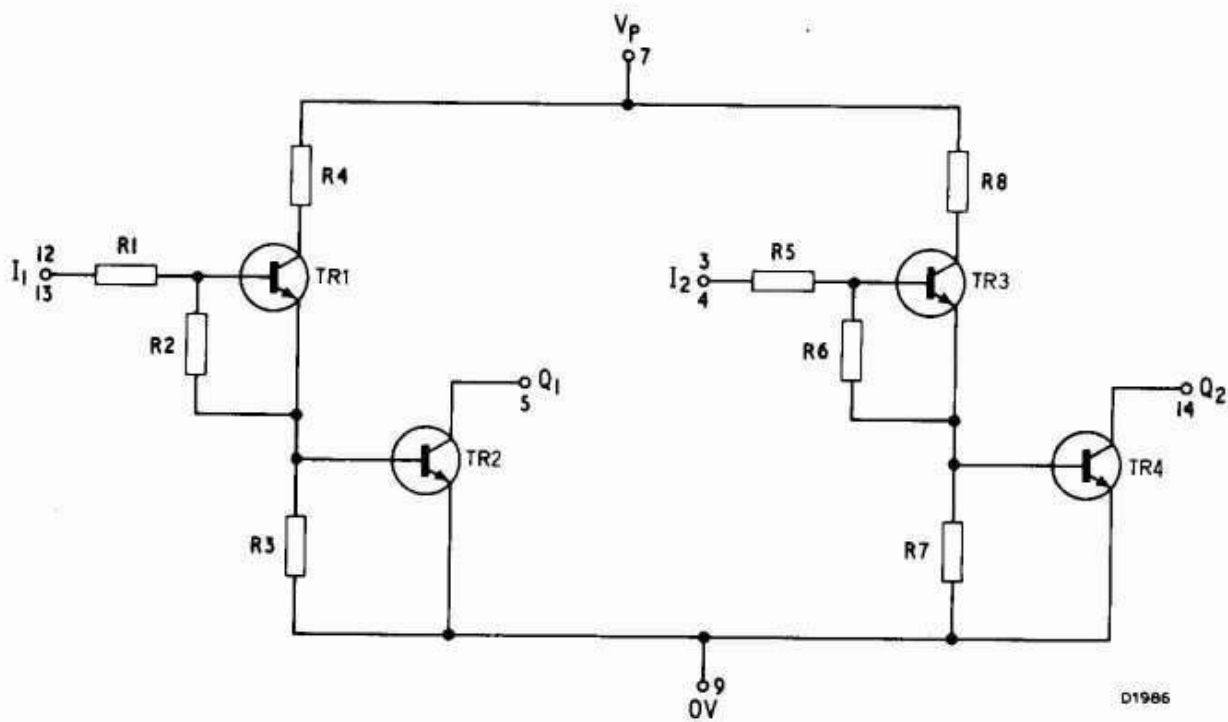
view from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Not connected	10	Not connected
2	Not connected	11	Not connected
3	Input to LPA 2 (I_2)	12	Input to LPA 1 (I_1)
4	Internally connected to pin 3 (I_2)	13	Internally connected to pin 12 (I_1)
5	Output from LPA 1 (Q_1)	14	Output from LPA 2 (Q_2)
6	Not connected	15	Not connected
7	Positive supply V_P (+)	16	Not connected
8	Not connected	17	Not connected
9	Common supply (0V)		

NORBIT 2 TWIN LOW POWER OUTPUT

2LPA60

CIRCUIT DIAGRAM



NORBIT 2 TWIN 4 INPUT NOR

2NOR60

This data sheet should be read in conjunction with
NORBIT 2 Series

DESCRIPTION

Two electrically independent 4-input NOR circuits. If any input of a NOR is at the '1' level, then the output of that 'NOR' will be at the '0' level.

COLOUR

Black

ELECTRICAL DATA

Power supply

Supply voltage, V_P	$+24 \pm 25\%$	$V_{d.c.}$
Supply current to pin 16 or 7	max. 4.8	mA ←

Input

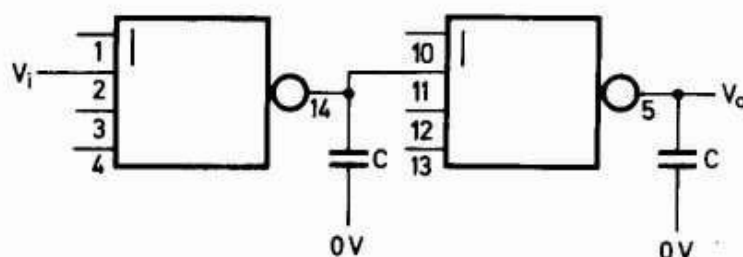
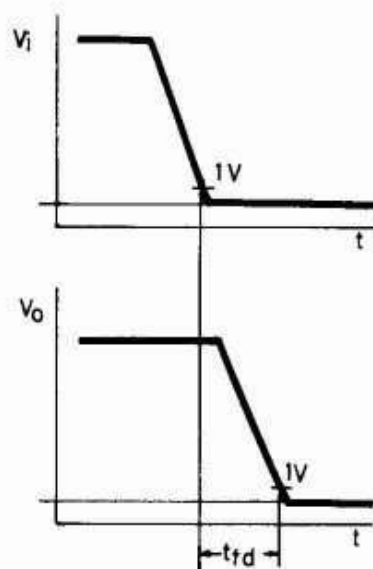
Logic '0'	0 to +0.3	V
Logic '1'	$+(0.24V_P + 7.2)$ to V_P	V
Loading per input	1	d.u.

Output

Loading per output	6	d.u.
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Propagation delay (t_{fd})

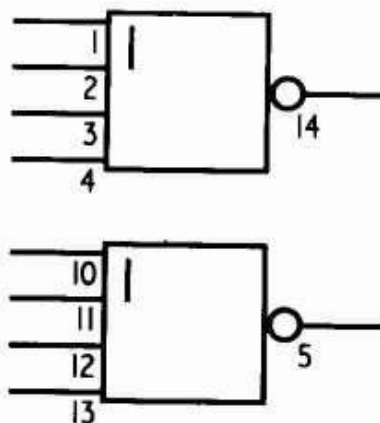
Over two stages	max. 6	μs
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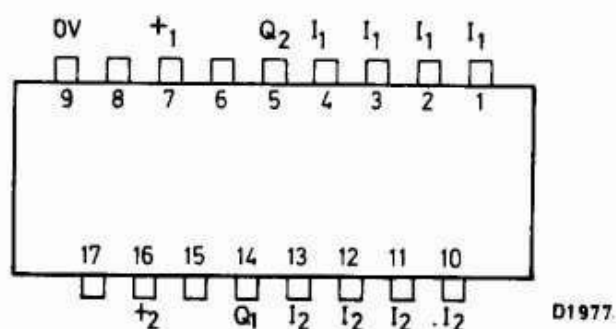
The delay time is defined as the time difference between the 1V points of the negative-going input and output voltages of two cascaded NOR's, each being loaded with 200pF.

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DRAWING SYMBOL



TERMINAL CONNECTIONS



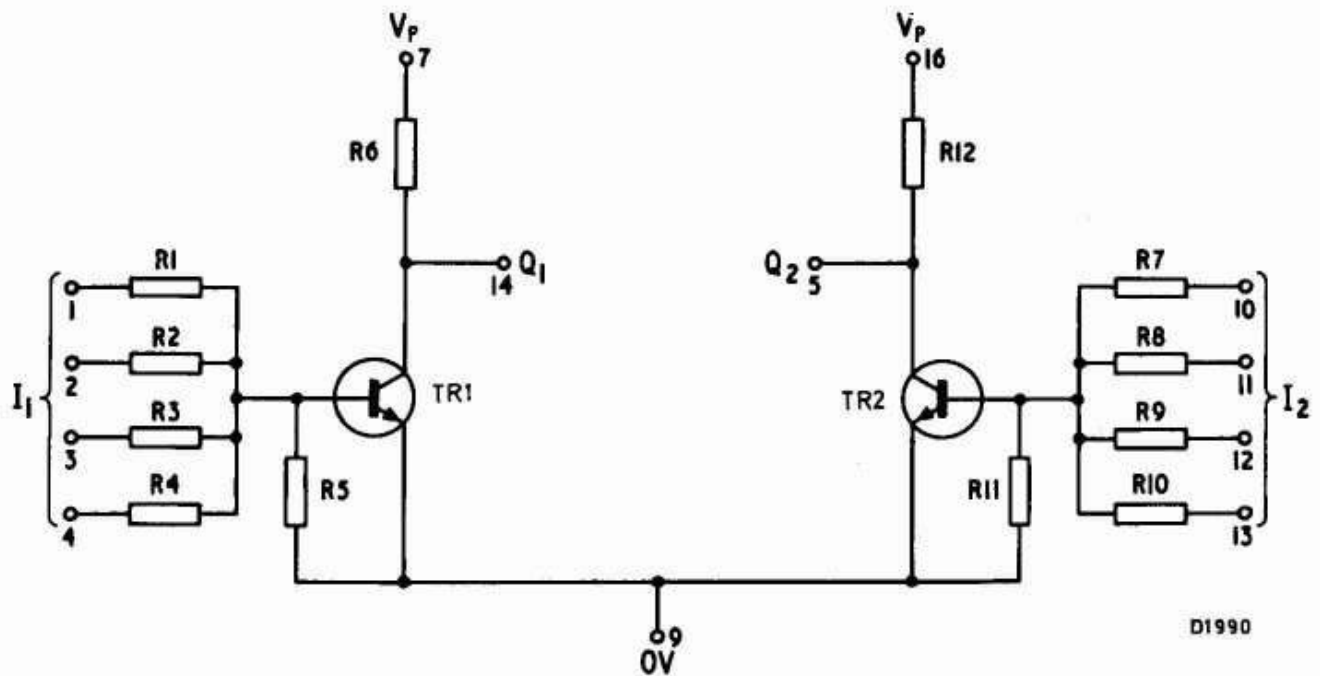
view from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Input 1 to NOR 1 (I_1)	10	Input 1 to NOR 2 (I_2)
2	Input 2 to NOR 1 (I_1)	11	Input 2 to NOR 2 (I_2)
3	Input 3 to NOR 1 (I_1)	12	Input 3 to NOR 2 (I_2)
4	Input 4 to NOR 1 (I_1)	13	Input 4 to NOR 2 (I_2)
5	Output from NOR 2 (Q_2)	14	Output from NOR 1 (Q_1)
6	Not connected	15	Not connected
7	Positive supply, V_P to NOR 1 ($+_1$)	16	Positive supply, V_P to NOR 2 ($+_2$)
8	Not connected	17	Not connected
9	Common supply (0V)		

NORBIT 2 TWIN 4 INPUT NOR

2NOR60

CIRCUIT DIAGRAM



This data sheet should be read in conjunction with
NORBIT 2 Series

DESCRIPTION

Two electrically independent filter circuits which may be used to suppress interference and eliminate the effects of contact bounce occurring on external switches, using an external capacitor. A high voltage is used to break down the contact film resistance of external switches.

COLOUR

Green

ELECTRICAL DATA

Power supply

The logic supply is not connected to the unit; the 0V terminals (pins 8 or 17) should be connected to the central earth point.

Input

Voltage for '1' out		+100 ± 25%	V _{d.c.}
Negative input voltage (under fault conditions)	max.	-100	V _{d.c.}
Current per input	steady, max.	3.5	mA
	surge, max.	4.8	mA

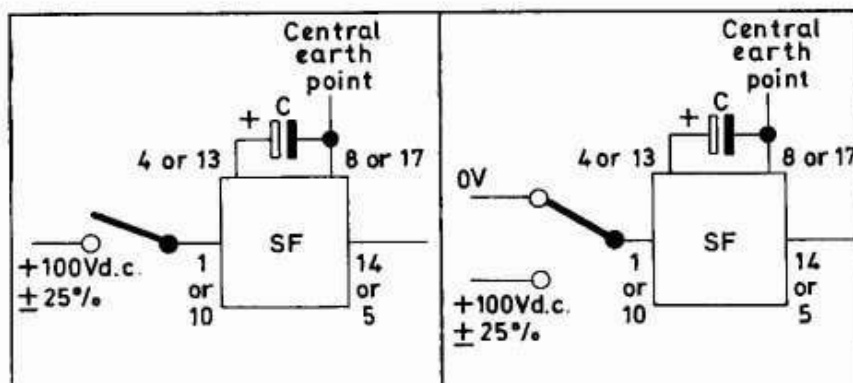
Output

Loading per output		2	d.u.
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The output will be '1' when the input has been applied for longer than the time shown under "Operation" below. Similarly the output will be '0' within the appropriate time also given.

Operation

The external capacitor (C) should be connected between the appropriate terminals C₁ and/or C₂ and the common 0V terminal. The use of a 64V electrolytic capacitor is recommended, and its value may be obtained from the formulae below.



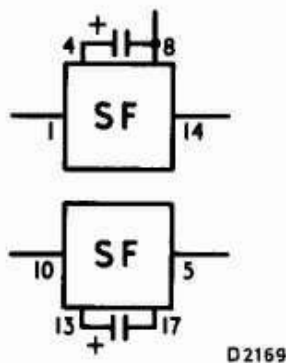
Type of contact		Single pole/single throw	Changeover
Tolerable contact bounce time	max.	$1.4C$ ms	$1.4C$ ms
Frequency of operation with 1:1 mark space ratio	max.	$\frac{6.3}{C}$ Hz	$\frac{10.6}{C}$ Hz
Time for which input must be applied to ensure '1' out	min.	$42C$ ms	$42C$ ms
Time for which input must be disconnected to ensure '0' out	min.	$26C$ ms	$18C$ ms

where C is the value of the external capacitor in μF

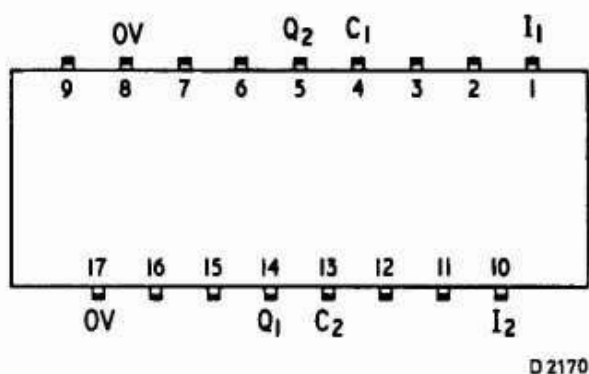
NORBIT 2 TWIN INPUT SWITCH FILTER

2SF60

DRAWING SYMBOL



TERMINAL CONNECTIONS

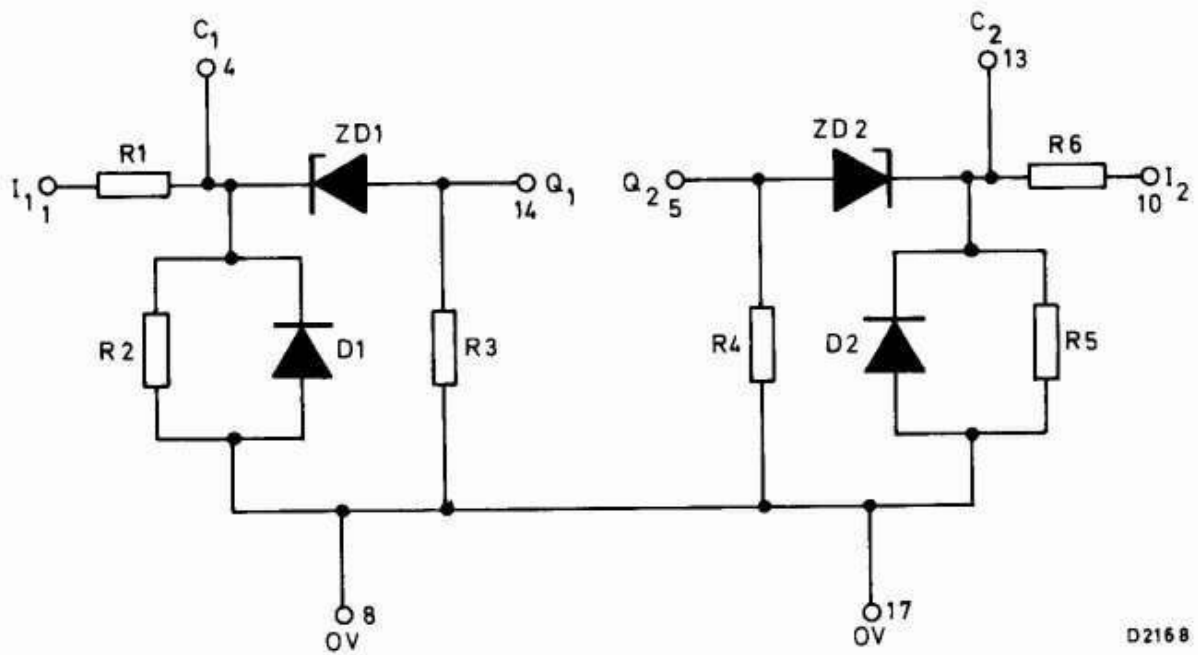


view from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Input to SF1 (I_1)	10	Input to SF2 (I_2)
2	Not connected	11	Not connected
3	Not connected	12	Not connected
4	External capacitor for SF1 (C_1)	13	External capacitor for SF2 (C_2)
5	Output from SF2 (Q_2)	14	Output from SF1 (Q_1)
6	Not connected	15	Not connected
7	Not connected	16	Not connected
8	Common supply (0V)	17	Common supply (0V) (internally connected to pin 8)
9	Not connected		

Mullard

CIRCUIT DIAGRAM



This data sheet should be read in conjunction with
NORBIT 2 Series

DESCRIPTION

Two gating circuits to perform extra independent trigger functions for use with the flip-flop FF90. The mode of operation is the same as for the trigger functions of the FF90. Switching is performed by applying signals to the trigger terminals T₁ and T₂ and these signals are controlled by the gates G₁ and G₂ respectively. The trigger terminals may be expanded by the addition of diodes to the terminals ET₁ and ET₂ to provide an 'OR' or inhibit facility. The extra resistor (R10), connected to terminal W₁, provides the 'set' facility for the FF90. The terminals EG₁ and EG₂ are not normally used.

COLOUR

Red

ELECTRICAL DATA

Power supply

Supply voltage, V _P		+24 ± 25%	V _{d.c.}
Supply current to pin 16	max.	21	mA ←

Input

Logic '0'	0 to 0.3	V
Logic '1'	+(0.24V _P + 7.2) to V _P	V

Loading

The 2TG90 introduces pulse logic to the NORBIT 2 range and, because of the circuits used, the ability of the driving block to accept current at the '0' level must be considered. This ability to obey the current and timing requirements is expressed simply in terms of 'z.u.'. Normal drive units, i.e., 'd.u.', must still be considered. The input requirements at the various terminals of the 2TG90 are given in table 1.

Table 1

Function	Input	d.u. '1' level	z.u. '0' level	Notes
Set (put Q_2 of FF90 to 1)	S	1	0	The 'set' input may be expanded by using up to 3 suitable diodes on each input. The cathode of each diode is connected to the input. If the 'set' facility is used, the input must be held at '0' (and not left open circuit) except during the input period.
Gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate.
Gate	G_1, G_2 via diode (Notes 1 and 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. The anode of the diode must be connected to the input
Trigger	T_1, T_2	0	2	Only a negative-going 1/0 edge occurring within $3\mu s$ provides the required signal. If T_1 and T_2 are interconnected, 4z.u. are required.
Trigger	ET_1, ET_2 via diode (Notes 1 and 2)	0	2	Only a negative-going 1/0 edge occurring within $3\mu s$ provides the required signal. If ET_1 and ET_2 are interconnected, 4z.u. are required. A maximum of two diodes may be connected to each ET terminal. The anode of each diode must be connected to the input.

NOTES

1. Suitable diodes are: BAX13 or BAX16.
2. When used, the external diodes should be mounted as close as possible to the twin trigger gate.

The loadings in d.u. and z.u. for the units in the NORBIT 2 range are given in table 2 below. The d.u. capability remains exactly as specified in the corresponding data sheets.

Table 2

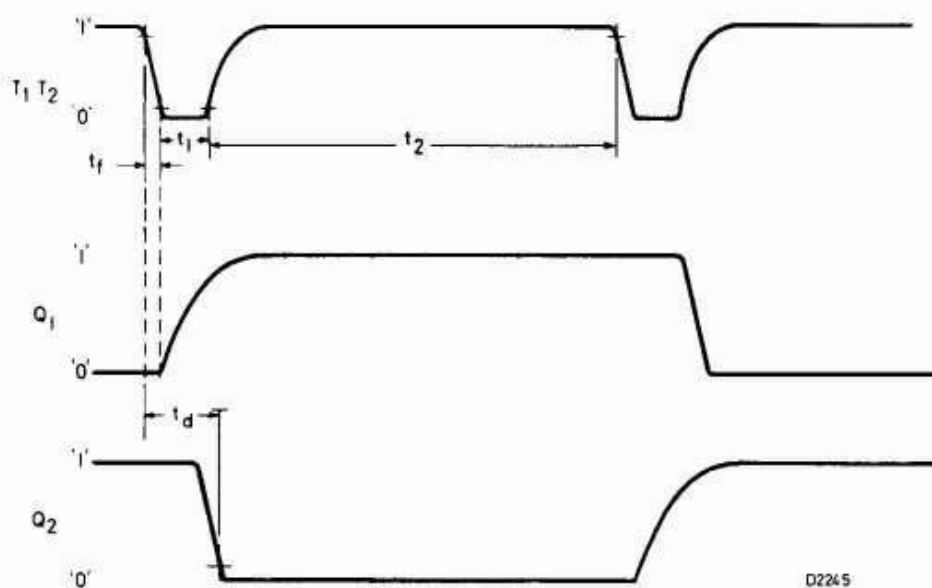
Unit	d.u. '1' level	z.u. '0' level	Notes
NOR of 2NOR60	6	12	2 inputs must be connected in parallel. Signal must be derived from a chain of units that includes either a PS90, an FF90 or a TU60.
2IA60 as low power output	20	50	Signal must be derived from a chain of units that includes either a PS90, an FF90 or a TU60. Both the inverting and non-inverting connections can be used, but pins 5 and 6 must be inter-connected.
NOR of 4NOR60	6	0	No z.u. available. Therefore, these units must not be used to drive a 2TG90 directly.
LPA60	-	0	
PA60 and HPA60	-	0	
TU60	5	0	
SF60	2	0	
PS90	6	40	
FF90	5	7	

Output

The outputs W_1 and W_2 are suitable only for use with one FF90; W_1 and W_2 should be connected to B_1 and B_2 respectively.

Inter-wiring capacitance max. 50 pF

To ensure this the 2TG90 should be mounted as close as possible to the FF90.



Operational requirements

The signal at the gate must be present for at least the duration of its recovery time before the triggering edge is applied to T_1 or T_2 . It is permitted to change the gate signal simultaneously with the triggering edge.

Fall time, t_f	max.	3	μs
Pulse duration, t_1	min.	5	μs

Maximum values in kHz for pulse repetition frequency at T terminals, $\frac{1}{t_1 + t_2}$, are given in table 3.

Table 3

Connection	$t_2 = t_1$	$t_2 = 10t_1$
Flip-flop with input applied to T_1 and T_2 connected together	5.0	7.0
Flip-flop with input to T_1 or T_2 , having ET_1 and ET_2 interconnected and with gate diodes as in table 1	5.0	12.5

Set pulse duration	min.	50	μs
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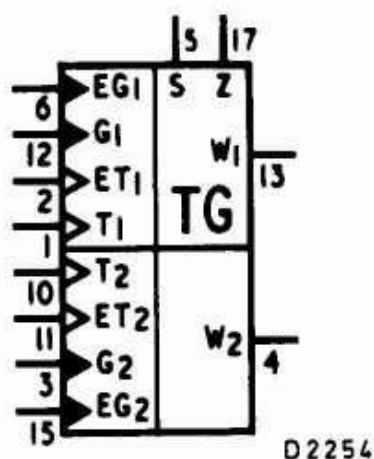
NORBIT 2 TWIN-TRIGGER GATE

2TG90

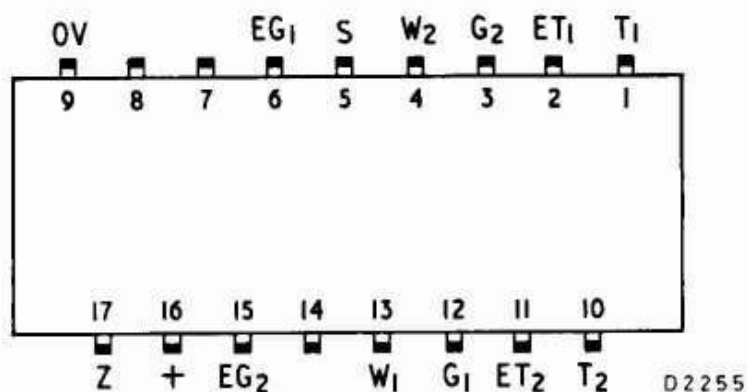
Characteristics

Trigger recovery time, t_2	typ.	73	μs
	max.	99	μs
Gate recovery time			
gate directly connected	typ.	105	μs
	max.	137	μs
with gate diodes	typ.	64	μs
	max.	77	μs
Switching delay, t_d	typ.	3	μs
	max.	8	μs

DRAWING SYMBOL



TERMINALS CONNECTIONS



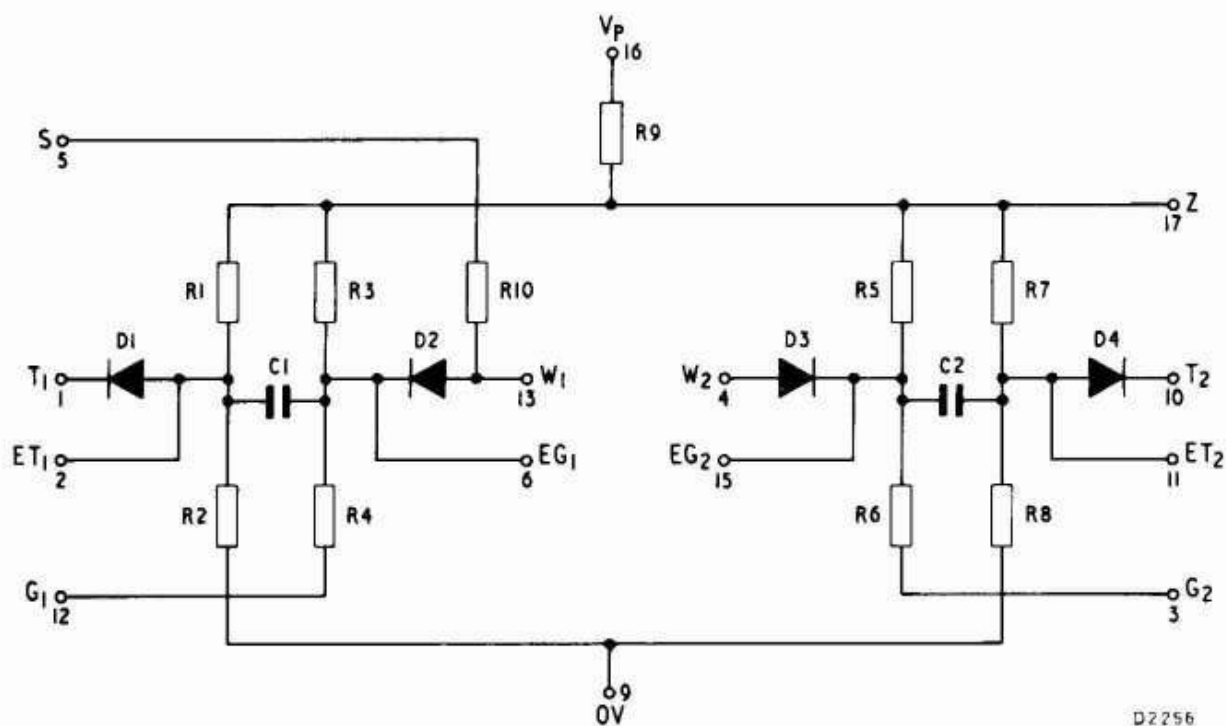
view from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Trigger input (T ₁)	10	Trigger input (T ₂)
2	Extension trigger input (ET ₁)	11	Extension trigger input (ET ₂)
3	Gate input (G ₂)	12	Gate input (G ₁)
4	Output to flip-flop pin 4 (W ₂)	13	Output to flip-flop pin 13 (W ₁)
5	Set terminal (S)	14	Not connected
6	Extension gate input (EG ₁)	15	Extension gate input (EG ₂)
7	Not connected	16	Positive supply, V _P (+)
8	Not connected	17	Voltage reference terminal (connected to pin 17 on flip-flop) (Z)
9	Common supply (0V)		

NORBIT 2 TWIN-TRIGGER GATE

2TG90

CIRCUIT DIAGRAM



NORBIT 2 QUADRUPLE NOR

4NOR60

This data sheet should be read in conjunction with
NORBIT 2 Series

DESCRIPTION

Two electrically independent 2-input NOR circuits and two 3-input NOR circuits. If any input of a NOR is at the '1' level, then the output of that 'NOR' will be at the '0' level.

COLOUR

Black

ELECTRICAL DATA

Power supply

Supply voltage, V_P		$+24 \pm 25\%$	$V_{d.c.}$
Supply current to pin 7	max.	4.8	mA ←
Supply current to pin 16	max.	14.4	mA ←

Input

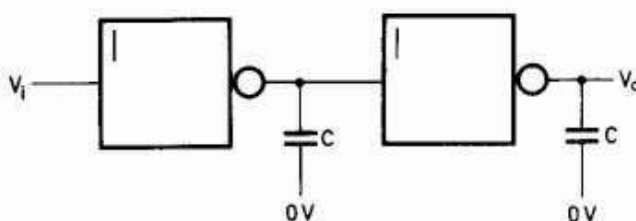
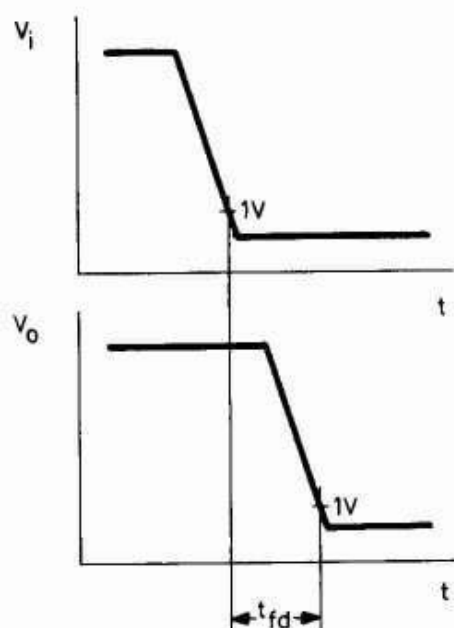
Logic '0'	0 to +0.3	V
Logic '1'	$+(0.24V_P + 7.2)$ to V_P	V
Loading per input	1	d.u.

Output

Loading per output	6	d.u.
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Propagation delay (t_{fd})

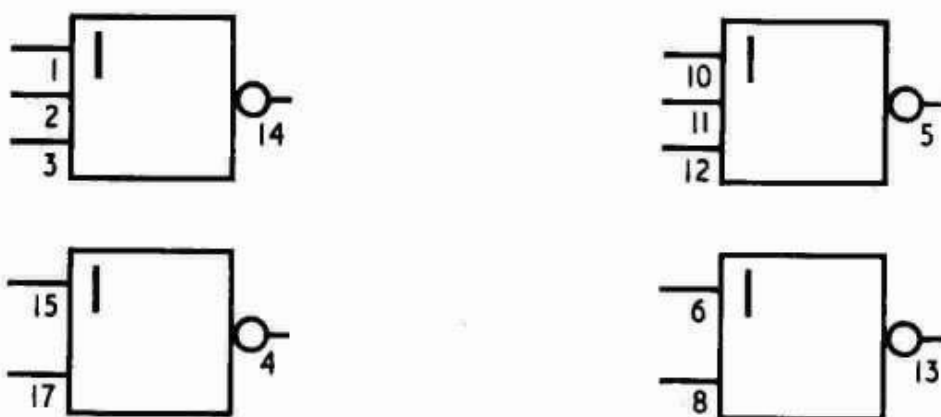
Over two stages	max.	26	μs
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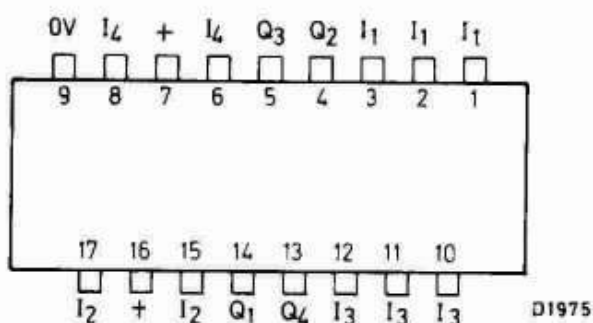
The delay time is defined as the time difference between the 1V points of the negative-going input and output voltages of two cascaded NOR's, each being loaded with 200pF.

Mullard

DRAWING SYMBOL



TERMINAL CONNECTIONS



view from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Input to NOR 1 (I_1)	10	Input to NOR 3 (I_3)
2	Input to NOR 1 (I_1)	11	Input to NOR 3 (I_3)
3	Input to NOR 1 (I_1)	12	Input to NOR 3 (I_3)
4	Output of NOR 2 (Q_2)	13	Output of NOR 4 (Q_4)
5	Output of NOR 3 (Q_3)	14	Output of NOR 1 (Q_1)
6	Input to NOR 4 (I_4)	15	Input to NOR 2 (I_2)
7	Positive supply, V_P to NOR 1 (+)	16	Positive supply, V_P to NOR 2, 3 and 4 (+)
8	Input to NOR 4 (I_4)	17	Input to NOR 2 (I_2)
9	Common supply (0V)		

CIRCUIT DIAGRAM

