Orton SC/MP Emulator plus NIBL

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Karen Orton 2019

Chapter 1 Emulator

Introduction

The Orton SC/MP emulator runs on a PIC16F877 and implements a cycle perfect emulation of an SC/MP microprocessor. There are limitations and the following are not supported:

1. Sense A interrupts
2. SIN and SOUT sense pin/flag
3. SC/MP bus control signals
4. The SIO instruction - behaves instead as 'shift right Extension'

Note that the emulation is 'cycle perfect' only in terms of instruction execution time. The bus structure and bus timing depart radically from the SC/MP specification.

The thirty-three PIC I/O pins provide the following:

Port pins	Function
RA0	Flag 0
RA1	Flag 1
RA2	Flag 2
RA3	(output, reserved)
RA4	Sense A
RA5	Sense B
RB0..RB7	D0..D7
RC0..RC7	A0..A7
RD0..RD7	A8..A15
RE0	/READ (NRDS)
RE1	/WRITE (NWDS)
RE2	(input, reserved)

The emulator can therefore address 64K of hardware memory with no external address latch being required. A bootstrap feature is included which permits up to 4K of SC/MP code to be written to low memory prior to execution of the emulator. This feature has been used to load NIBL BASIC. This code is write protected i.e. the first 4K of SRAM behaves like ROM.

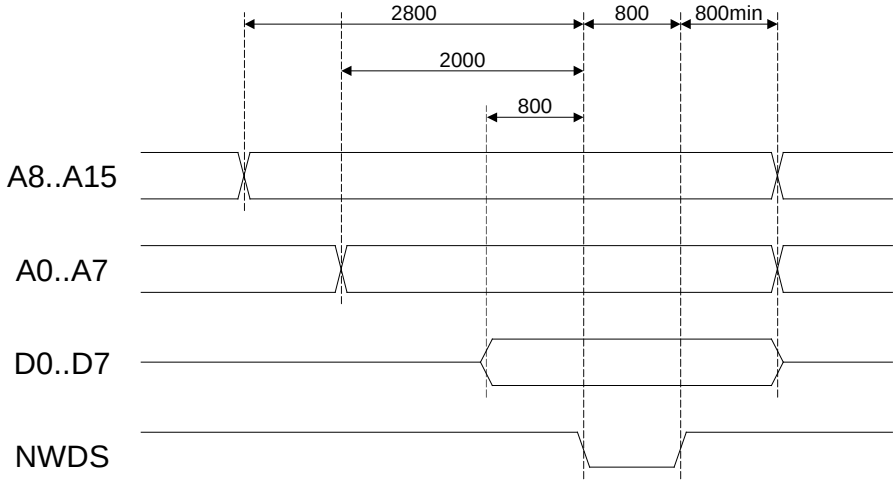
The PIC clock can be chosen in accordance with the speed of the SC/MP to be emulated:

PIC crystal	Equivalent SC/MP crystal	SC/MP machine cycle
10MHz	2MHz	2 µsec
20MHz	4MHz	1 µsec

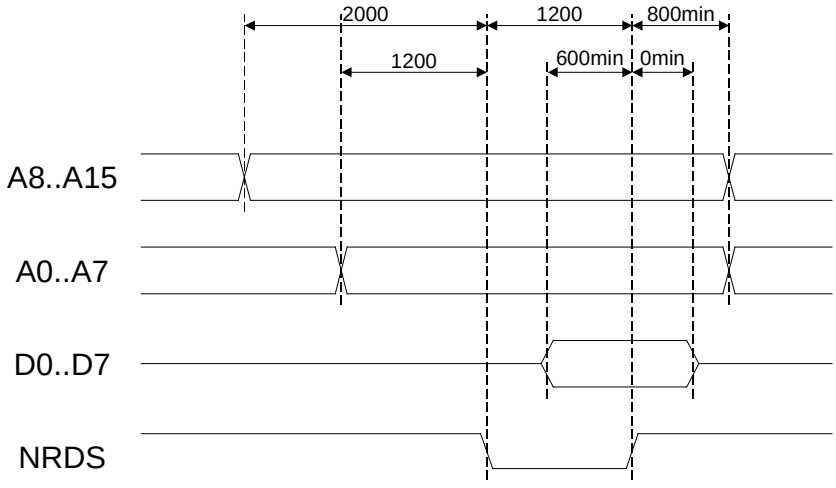
Chapter 2 Emulator bus timing

These timings are for a 4MHz SC/MP emulation (20MHz PIC crystal) and are in nanoseconds (ns). These figures should be doubled for a 2MHz SC/MP emulation. Regardless, the bus timings are very sedate and almost any speed of SRAM should work reliably with the emulator.

Write cycle



Read cycle



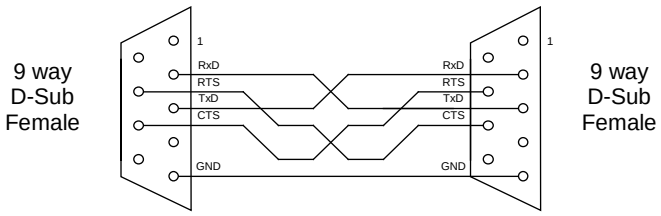
Chapter 3 NIBL BASIC Connection

An SC/MP computer running NIBL BASIC can be created with the addition of an SRAM. NIBL traditionally interfaced to a teletype using the following flag and sense pins:

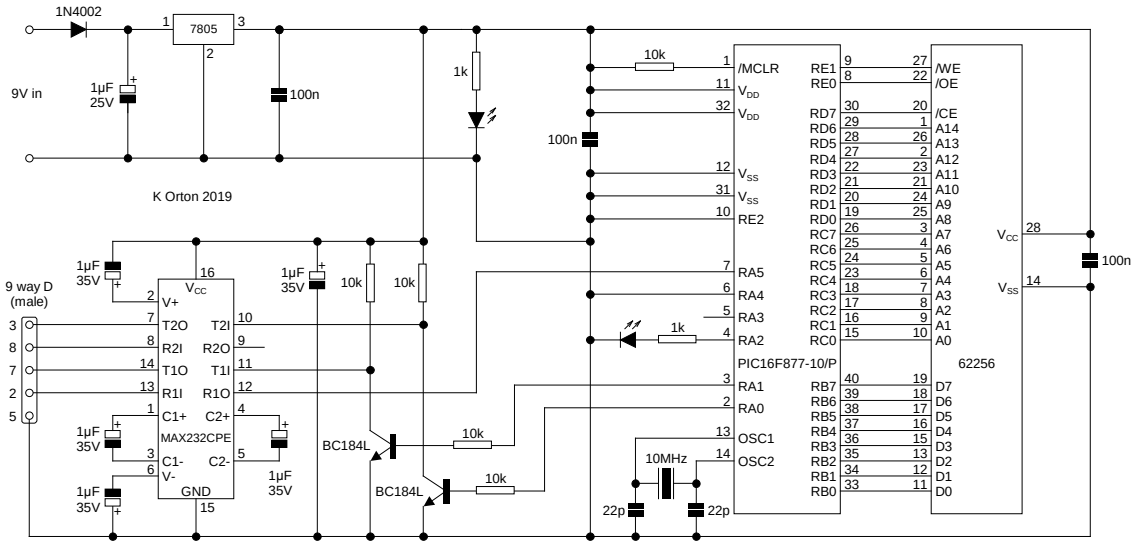
Flag/sense	Function	Comments
Flag 0	110 Baud serial data out	Inverted by present day standards
Flag 1	Reader relay	Can be used as an RTS signal, though again this signal is inverted
Sense B	110 Baud serial data in	Correct polarity!

Use of the reader relay signal (Flag 1) as an RTS flow control signal is not guaranteed to work in all circumstances. To work successfully, the terminal or computer to which the SC/MP computer is connected must be able to respond IMMEDIATELY to assertion of RTS (actually, CTS by the time this flow control signal reaches the connected device). Not all communication adapters can do this.

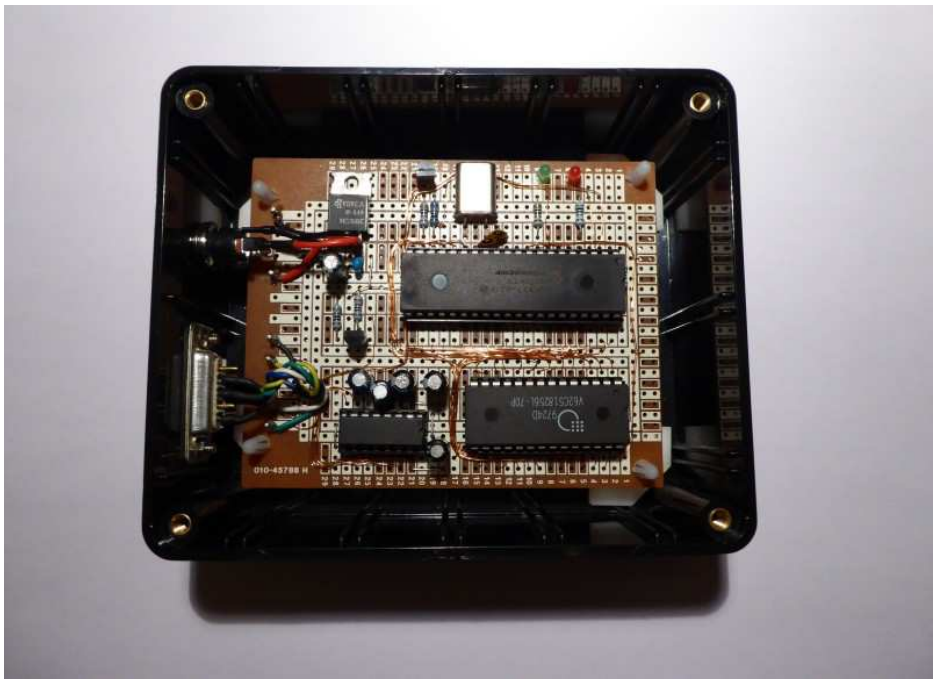
The supplied NIBL computer circuit (see Chapter 3) presents a 9 way male D-Sub connector which provides a DTE connection. This can be connected to a PC COM port by use of a five wire cross-over ('null modem') cable:



Chapter 4 Hardware



Chapter 5 Photo



Chapter 6 Software

There is one supporting file associated with the Orton SC/MP emulator:

File	Purpose
SCMPemu.asm	The SC/MP emulator PIC firmware