27-29MHz CONVERSIONS

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uring the last few years, a variety of techniques have been published corporating suggested methods of onverting the frequency ranges of latively cheap FM CB transceivers om the CB frequencies to the 29.3-29.7 nateur FM allocation. The large crease in occupancy of the 144/146MHz nd has meant that the availability of a rther band capable of reliable short nge communication, such as local gchew nets or short range mobiles, ould be an advantage.

n the present condition of the sunspot cle the 28MHz band meets the above quirements admirably, and with the casional opening offers an added petus to the adventurous. The FM ocation is normally 29.3-29.7MHz, but use of 29.3-29.5 as a satellite downlink nd means that most activity is centred the 29.5-29.7 region. The use of dified, cheaply available CB transvers, together with the associated cillary fittings such as aerials, etc, ers a simple and inexpensive method aking advantage of this situation.

approaches

ne techniques advocated have eloped into two broad avenues of roach.

rstly, variation to the switched count ge applied to the PLL, so that the oded signal can be varied outside the normally accepted range and thus give extended coverage. This extension can be achieved by either:

(i) Modifying the count range by switching, or by wiring alterations to the code line.
(ii) The use of binary adders to pre-load the count line.
(iii) Variations to the offset frequency.

Alternatively, substitution of a dedicated device by a binary controlled PLL, and by using an Eprom in the normal BCD program line to convert to a straight binary code. In the case of FCC-coded switch lines, the Eprom can also be programmed to by-pass the guard channels and to take out the channel 22/23 switch around.

The common form of straight binary input PLLs have one shared characteristic: the 'divide-by-N' counter on the program lines usually has a limited count range and is incapable of counting faster than about 2.5 MHz.

This is the reason for the mixing technique adopted where the 10.240MHz reference frequency is firstly divided by 1024 to give the 10KHz channel separation control, and also by two to give a 5.12MHz output. The 5.12MHz output is then multiplied to 15.36MHz, and this so-called 'offset frequency' is then mixed with the VCO operating in the 17MHz region to give an output around 1.6MHz. This 1.6MHz is applied to the counter and divided down to 10KHz before comparing with the 10KHz reference.

The 17MHz is then mixed with the 10.240, which has had 455KHz offset added to it by suitable count variation controlled by the Tx/Rx switch, to give a 10.695 + 17MHz mix for the transmit frequency, or the 17MHz only is used as first oscillator injection to give a 10.695 first IF, which is then mixed in the second oscillator with 10.240MHz from the reference crystal to give a 455KHz second IF. To convert to 29.3MHz, the 15.36MHz frequency could possibly be altered to 16.9, which will cause the VCO to be shifted to 19MHz and thus give 29MHz operation (in the case of 27.6/27.99 equipment).

Prevention

To prevent the normal CB fan from converting his set to operate outside the 26.950/27.450 range, the FCC required that all PLLs be non-transferable, resulting in a new family of devices being created in which the count range in the chip could not be varied. The count range was pre-programmed into a Read Only Memory, and activation or access to this memory was only made possible by a dedicated program input in BCD, *not* by a straight binary. Any other inputs were illegitimate and were considered by the device to be a miscode.

The program used on the LC7137 device currently in use in the UK for sets is shown in *Figure 1* (note Tx is to be multiplied by 10).

Many forms of this dedicated device were produced, and this type of circuit meant that the transceivers were no longer capable of being transferred to different frequency ranges without replacing the complete synthesiser network, a technique widely adopted in the UK to convert former pirate sets to the licensed range set up by the British Home Office (27.601-27.991MHz).

ROM

In effect this means that the divide-by-N value is no longer determined by the program lines, but by the ROM. The program lines act only as an instruction to the ROM to release a certain group of numbers from its store, this group of numbers being the required discrete count or divide ratio. Since a 6-bit binary coded decimal line is used the limit is to a count of 40, so variation to the input cannot be a practical possiblity. Any other code input is read as a miscode and ignored by the ROM in any case.

1 Showing program data and division code

Program Code						Rx(x5)	Tx (x10)
D1	D2	D3	D4	D5	D6	(TR - 1)	(TR - 0)
1	0	0	0	0	0	3381	2760
0	1	0	0	0	0	3383	2761
1	1	0	0	0	0	3385	2762
0	0	1	0	0	0	3387	2763
1	0	1	0	0	0	3389	2764
0	1	1	0	0	0	3391	2765
1	1	1	0	0	0	3393	2766
0	0	0	1	0	0	3395	2767
1	0	0	1	0	0	3397	2768
0	0	0	0	1	0	3399	2769
1	0	0	0	1	0	3401	2770
0	1	0	0	1	0	3403	2771
1	1	0	0	1	0	3405	2772
0	0	1	0	1	0	3407	2773
1	0	1	0	1	0	3409	2774
0	1	1	0	1	0	3411	2775
1	1	1	0	1	0	3413	2776
0	0	0	1	1	0	3415	2777
1	0	0	1	1	0	3417	2778
0	0	0	0	0	1	3419	2779
1	0	0	0	0	1	3421	2780
0	1	0	0	0	1	3423	2781
1	1	0	0	0	1	3425	2782
0	0	1	0	0	1	3427	2783
1	0	1	0	0	1	3429	2784
0	1	1	0	0	1	3431	2785
1	1	1	0	0	1	3433	2786
0	0	0	1	0	1	3435	2787
1	0	0	1	0	1	3437	2788
0	0	0	0	1	1	3439	2789
1	0	0	0	1	1	3441	2790
0	1	0	0	1	1	3443	2791
1	1	0	0	1	1	3445	2792
0	0	1	0	1	1	3447	2793
1	0	1	0	1	1	3449	2794
0	1	1	0	1	1	3451	2795
1	1	1	0	1	1	3453	2796
0	0	0	1	1	1	3455	2797
1	0	0	1	1	1	3457	2798
0	0	0	0	0	0	3459	2799
						NOTE: All odd numbers	

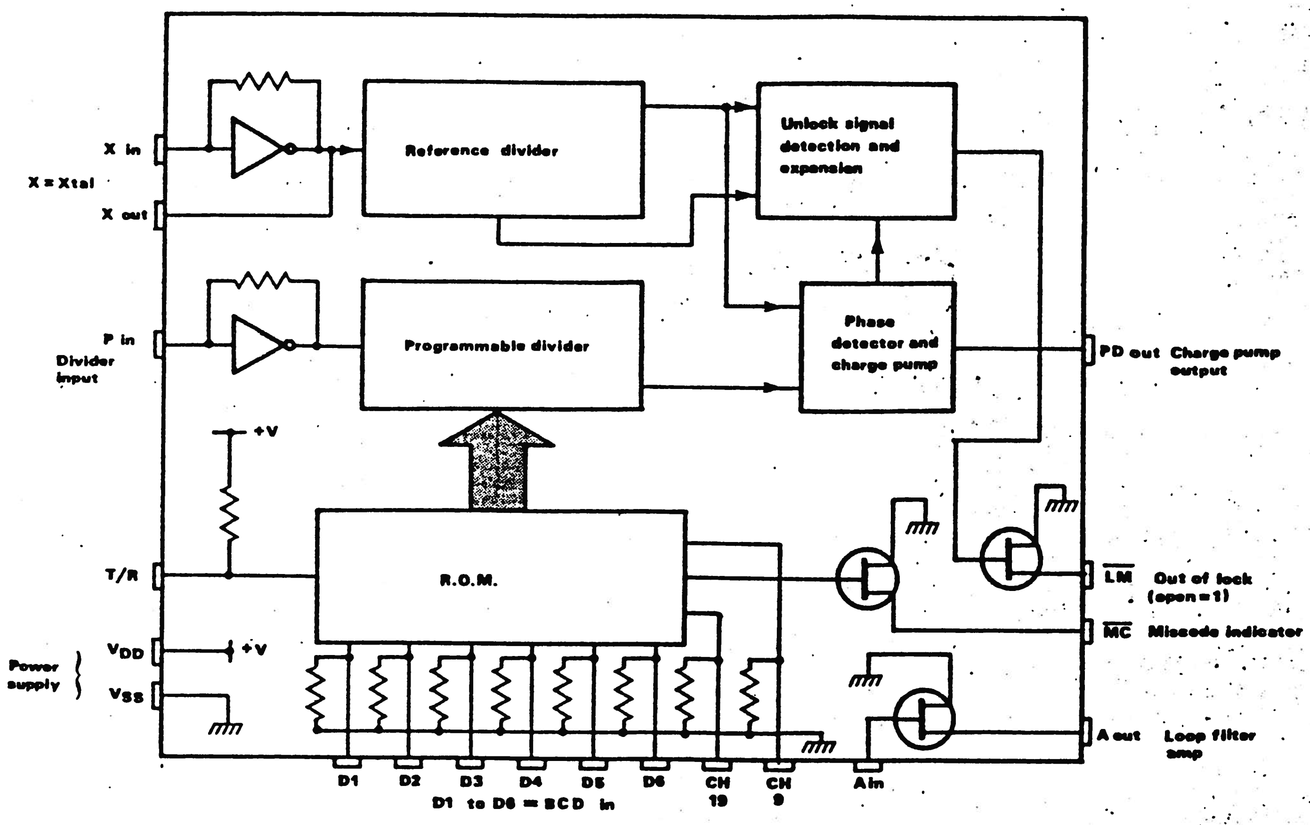

Fig 2 LC7137 block diagram

Examination of the structure of the device *(Figure 2)* shows some interesting features. Firstly the divide-by-N section, which is controlled by the ROM in its instruction phase, is now capable of dividing up to a 22MHz count range and is therefore capable of reading the VCO input directly. Whilst this offers certain advantages, which will become apparent later, the obvious disadvantage is that methods of varying the offset are no longer applicable.

One other interesting point is that the divider ranges operate at two levels *(Figure 1)*, meaning that the VCO will be operating at quite different frequencies in the transmit and receive modes. The frequency arrangements used on receive are in multiples of two and are in an odd number sequence, whereas the Tx codes are in single number progression.

The actual arrangements chosen in the 7137 are to divide the VCO frequency directly by a discrete number, giving a 10KHz value on lock, whereas the VCO on receive operates on a frequency of 'Required frequency – 10.695MHz', but is counted in 5KHz steps using two steps per division. Since the desired frequency after division is 10KHz for reference, and the second IF is 455KHz, ie 45.5 x 10, then it is apparent that 45.5 is not a realisable count value and 45.5 x 2 = 91 is used. In order to bring the odd 5KHz back into the 455, the frequency is offset by the odd number used in the count chain.

From the discussion to date it would appear impossible to vary the frequency range covered by the device, since the phase lock circuit uses a 5 or 10KHz comparison frequency, as the circuit requirements dictate. The only possible variable is the VCO input, and here advantage may be taken of the wide lock-up range of the device.

Outside control

As mentioned earlier, the input range of the divide-by-N or programmable counter extends to some 22MHz (specification states in excess of 16MHz, but all samples checked so far have gone in excess of 21MHz). The method of attack adopted was to influence the device into operating in a different frequency range by bringing a degree of outside control onto the programmable counter.

Assuming that a further divide-by-2 is introduced into the 1024 fixed reference divide, so that the reference frequency is now 5KHz, and that the incoming VCO frequency is the determinant value, the procedure adopted is to present the programmable counter with a frequency which, when divided down, would not give a 5KHz frequency to the phase comparator. The comparator senses an out-of-phase situation and creates a correction voltage which is applied to the VCO, varying the VCO frequency until the divided value is exactly 5KHz, i.e. until the circuit is in lock.

If some method of varying the VCO frequency between leaving the VCO and arriving at the phase detector in its divided form could be derived, the possibility of misleading the device into operating on a different frequency range could be created.

The sequence of operations of the frequency count in the programmable divider is for the divider gate to be opened for a certain period of time, and a train of pulses to be loaded into its register. These stored pulses are then counted down by division at a programmed rate, and the resultant passed to the comparator. The gate time period is set by the 10.240MHz crystal, so it is a fixed time which cannot be varied inside the device.

In order to present a difference in output, variation in the input frequencies must occur. If wide variations are required the range may exceed the electrical parameters of the device, since a certain limited range of lock-up is characteristic of any one device. The only method of variation is to control the programmable counter gate opening time from an outside source, thus varying the number of pulses allowed to enter.

The method adopted was to institute a

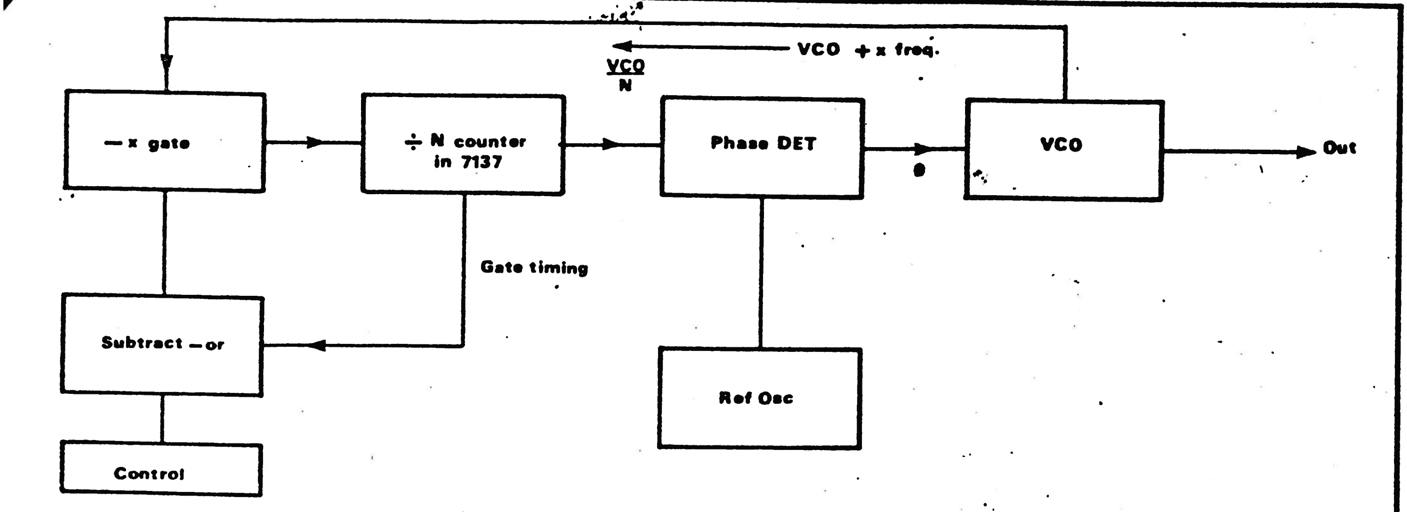

Fig 3 *Basic outline of technique*

	Rx Division	Tx Division	Rx Local Osc Freq	Tx Output Freq
	3441 (x 5KHz) If we prevent 340 pulses from entering device we effectively increase count by 340	2790 (x 5 x 2KHz) If we prevent 170 pulses from entering device we effectively increase count by 170	17205KHz (3441 x 5)	27900KHz (2790 x5 x 2)
lHz ge	3441 340 ——— 3781 x 5 18905 10695 + (IF) ——— 29600	2790 170 ——— 2960 x 5 = 14800 x 2 = ——— 29600	18905KHz	29600KHz

Fig 4 *Values adopted for the UK variation of the 7137*

ı of subtraction in which the incom- frequency to the divider was ırently reduced in value, thus caus- he phase detector to take corrective ɔn by increasing the VCO frequency :ompensate for the amount sub- :ed.

r example, if the VCO was running in at 17MHz and the VCO frequency ally fed to the divider was only Hz, then the phase detector would ɜase the VCO frequency to 18MHz ıat the expected 17MHz frequency d then be applied to the comparator. inciple, what then happens is that a situation can only be achieved ı a 17MHz program number creates 18MHz VCO frequency, ie zero ıge on the PD output line. Basically, ɔhase detector is being fooled into ɜving that it is reading and rolling a 17MHz signal, whereas act it is controlling an 18MHz lator.

ɜ simple technique is outlined in *re 3*, and it can be seen that the ıod used is to close the input to the rammable counter for a finite frac- ɔf the permitted gate opening time, thereby only permitting the VCO frequency to be stored in the memory of the divider for a controlled fraction of the gate opening time.

This means that the actual number of pulses available for counting in the period is now reduced in proportion to the reduced time of the gate opening period. By varying the open time throughout the actual available time, a degree of control over the precise frequency measured is established, and by incorporating varying times a wide control of frequency variation can be introduced. An indication of the numerical values adopted for the UK variation of the 7137 is shown in *Figure 4.*

To introduce the required Tx offset for repeater use, it is only necessary to change the 170 pulse stop to 160 so that the transmit frequency is reduced to 29500KHz, or to 180 for 29700KHz.

Technical problems

The approach as suggested is simplicity itself, but the creation of the required circuitry presented many technical difficulties. Obviously mixing techniques can be ruled out in face of the impossible task of filtering out unwanted products, and a simple arithmetical subtractive technique had to be developed.

Timing

One essential feature was the timing of sequences. Since the synchronization of gate opening times and initiation of subtract frequency generation was vital, the problem of propagation delay or varying transit times in the circuitry involved created difficulties. High speed logic circuitry operational at the frequencies involved was not available initially, and eventually a system was developed in which the incoming train of pulses from the VCO was stopped at a logic gate until sufficient time had elapsed to permit a pre-determined number of pulses to be generated in a separate but synchronized encoder.

The time permitted as a gate closure time was that period of time necessary for a skip-ten counter and associated circuitry to count down from the loaded pre-determined value to zero. At this point the gate opened and the programmable counter in the LC7137 took over. By this means only the remaining portion of the VCO train, ie the total originally available less the count in the loaded counter, was presented to the PLL.

The simple form of this operation is shown in *Figure 4* in crude form. To further elaborate on the technique, *Figure 5* shows the more detailed approach, and is the block diagram of the final solution to the problem.

The initiation of a train of pulses into the 7137 triggers the external counter, and immediately clocks the variable division generator and closes the gate. When the external counter has reduced the values stored in the encoder to zero, the gate is opened and the remaining time is used by the LC7137 to count the pulses arriving from the VCO.

Obviously the time is insufficient for a complete count, and the shortened number causes the phase detector to take corrective action and increment the VCO. The circuit technique adopted (*Figure 6*), was to use a count-by-ten skip counter which is controlled by a pulse derived from the 7137 starting signal. Whilst running, this counter will maintain a logic 'one' at its output.

Pulses

The starting signal was originally derived from the phase detector output to the VCO, which was found to have sharp pulses on the line (*Figure 7*). These are normally filtered out in the loop filter but can be detected at the PD output from the device.

The pulses are used to switch a counter set with a divide ratio of either 34, 17 or 16 depending on the function required, this selection being made by the Tx/Rx or repeater offset switch. This counter is set to count down from the loaded values and at each count a pulse is applied to the free running divide-by-ten counter. Upon the low range counter reaching zero, the divide-by-ten counter stops and its output reaches a logic 'zero'.

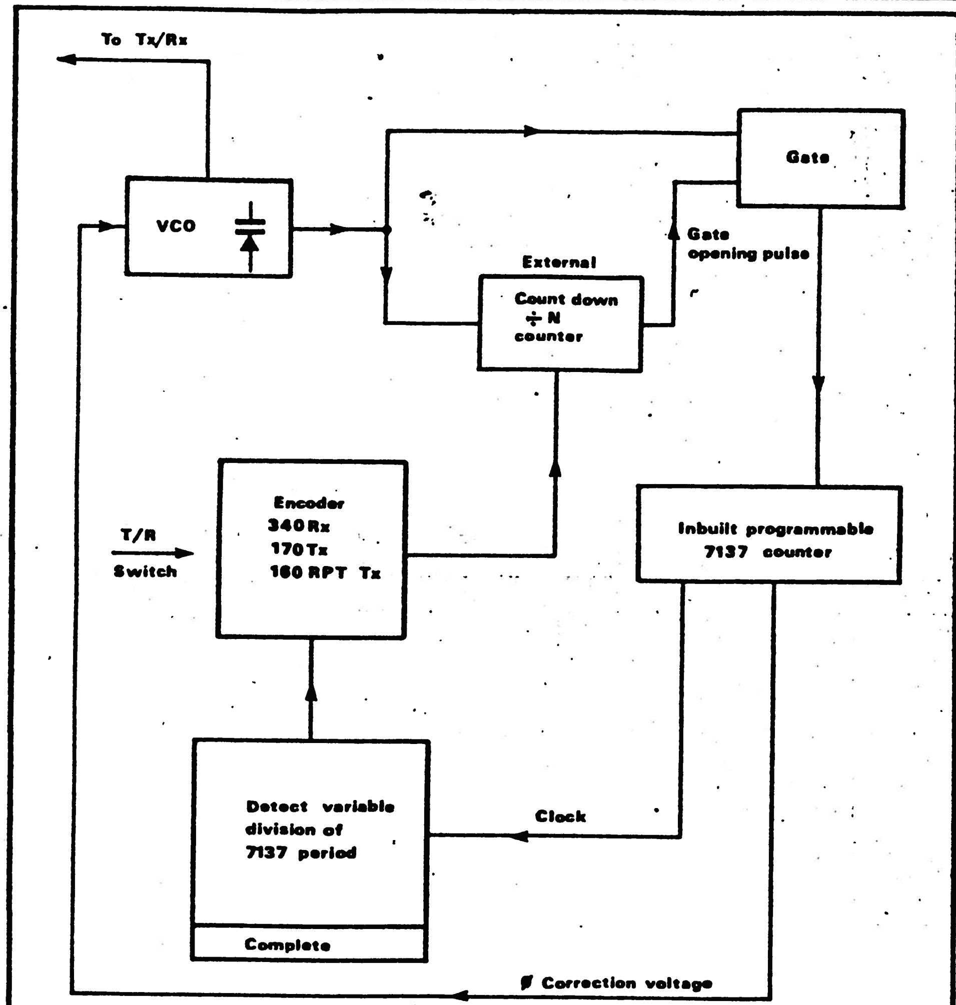

Fig 5 *Elaboration of the outline in Figure 3*

The output from the divide-by-ten counter controls a gate in the VCO feed to the 7137 so that the gate is closed when the 34 x 10 or 17 x 10 sequence is in operation, but opened immediately the zero is reached. The gate opening period only permits a reduced number of pulses to be registered by the 7137 before the next cycle commences, and consequently the phase detector takes corrective action.

The problems encountered were mainly with the signalling of the initiation. The pulse polarity met at the PD output was not constant, so a discriminator has to be incorporated. The loop filter

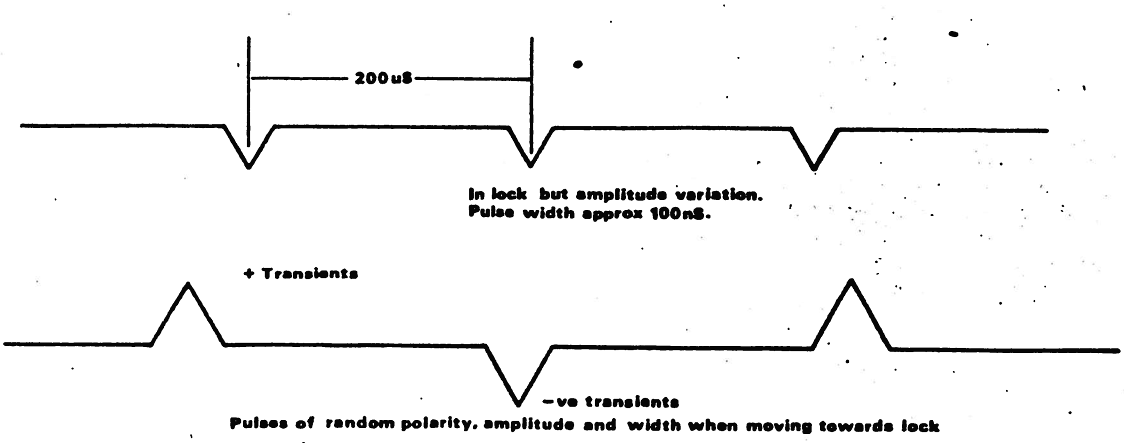

Fig 7 *Variations in the signal used for synch*

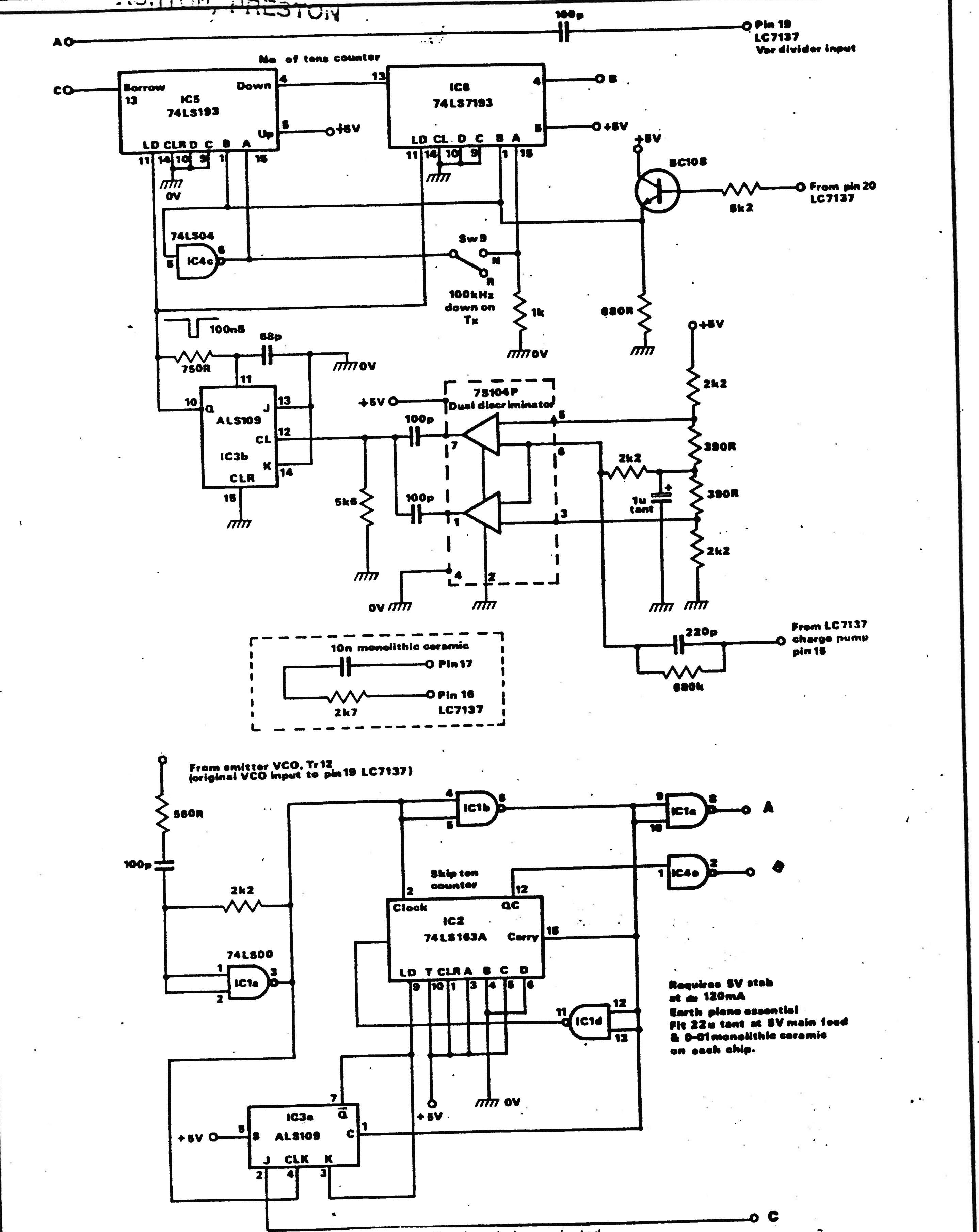

Fig 6 Circuit technique adopted

circuits in common use were not adequate and required a considerable enhancement in performance, since the lock-up time is proportional to the loop frequency limit, and it was found necessary to reduce this limit considerably. A later technique (not shown on circuit) was to extract the pulse from the reference frequency oscillator.

Further investigation permitted the use of the 10.240KHz reference crystal oscillator as a clock.

The system has been used on a number of UK FM CB transceivers with successful results. Repeater stations in the US and Germany have been activated and good DX contacts made from mobile CB type aerials and either barefoot or with a modified 25watt CB linear.

Sequence

Following the circuit diagram the actual sequence is as follows:

(a) To stop 340 pulses it is necessary to stop 34 x 10 pulses. Using the circuit as shown this means that IC1, IC2 and IC3a have to operate at speeds near the limit of the logic family chosen, yet even so gate propagation times are borderline.

(b) The incoming VCO frequency is applied to IC1a. The 2K2 resistor raises the gate into its linear region so that the amplitude of the input wave is increased and the input is to a certain degree squared up. The output of IC1a becomes the master clock for the skip-ten counter section, via IC3a.

(c) In the absence of a load pulse at IC2 pin 9 (low), IC2 counts until a carry appears at pin 15 (high). This is inverted by IC1d which disables the count enable (pin high – count, low – disable). The counter stays in this state (15) until a load pulse appears.

(d) Whilst the carry is high IC1c allows VCO pulses to pass to the LC7137 variable divider input. When the input to IC1c is low no pulses will pass.

(e) The logic diagram in *Figure 8* shows the operation of the skip-ten counter. It will be noticed that the QC output is used to decrement the number-of-tens counter. Eight clock intervals (400nS) are available for IC5 and IC6 to settle before IC3a detects if another skip-ten count is required.

(f) IC3a generates a low load pulse for one clock period only if IC2 carry is present, and if the J input is high. The J input only goes low and stays low if the number-of-tens counter reaches zero. A trigger from IC3b is needed (total countdown complete) to load a non-zero value into IC5. IC6 (Rx 34, Tx 17 or 16).

Note that the input weighting D = 8, C = 4, B = 2, A = 1 is used (*Figure 9*).

(g) The transistor buffers the Tx/Rx signal from the LC7137 Tx = O, Rx = 1. The gate IC4c inverts this signal and the connections used to the 'set' inputs of IC5 and IC6 (IC6 is the least significant counter) give the binary equivalents to 34, 16 or 17.

(h) IC3b is used as a 100nS monostable for each count complete signal at its input.

(i) The overall action is therefore as follows:
LC7137 variable divider count complete, load a value into IC5 and IC6, skip-ten counter operates until IC5 and IC6 reach zero, no further pulses stopped until LC7137 variable divider count is complete, when cycle is re-initiated.

DEC	QD	QC	QB	QA	
15	1	1	1	1	Waiting for low at pin 9. IC1c passing VCO frequency.
15	1	1	1	1	Low received (J on IC3a high next clock Q low further clock Q high).
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	Number of tens counter decremented.
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	Two pulses allowed through from VCO. If tens counter not yet zero
15	1	1	1	1	then another skip ten cycle begins.
5	0	1	0	1	
15	1	1	1	1	Total count of tens now complete. The removal of, say (Rx = 340 counts) in a 5KHz reference period is now complete. Another cycle is initiated by the next pulse detector trigger pulse.

Fig 8 *Skip 10 counter operation with number of tens counter*

Function	DEC	IC5	IC6
		DCBA	DCBA
Receive	34	0010	0010
Transmit	17	0001	0001
Repeater Tx	16	0001	0000

Fig 9 *Loading of IC5 and IC6*

Problems

One problem encountered was the occasional spasmodic operation of the initiating pulse circuitry due to the random nature of the polarity of the pulse (*Figure 7*), and also variations in the pulse width. Considerable variations to the loop filter proved that this could be overcome, except in odd versions of the LC7137. A modified circuit has already been mentioned in which the pulse was extracted from the reference oscillator, and this completely removed the problem.

The actual conversion is a relatively simple operation since only one track break is required, then five connections to the board are made and the installation is complete.

Board design demanded an adequate earth plane, and separation of certain circuit sections was essential. By adopting careful layout no screens were required, but good earths are essential.

FM quality

The quality of FM produced was quite good when the normal CB modulator circuits were used. In cases where conversion of an AM is required, a board containing a suitable modulator with built-in processor together with a 455KHz discriminator is available, and this mod is capable of very high quality transmission and excellent reception.

The above techniques may be used in a variety of circumstances and are not limited only to CB conversions.

In the case of the guard channels in the FCC arrangment of frequency allocation, it is suggested that channels 21 – 40 are used and the only variation is then the switch at channel 23, ie 29.500 – 29.700 = ch 21 – 40.

The installation does require a certain degree of care since the high frequencies involved are sensitive to strays. Normal installation technique is to mount the board perpendicular in its short length to the main board, and to install it with the earth face of the board to the rear of the transceiver.

Further development

The above discussion leaves a considerable field of further development to the keen experimenter and the writers would be interested in suggestions for other applications. REW