PET NOP TESTER

PURPOSE:

Test the address lines through out the main logic pcb.

HARDWARE:

One MOS 6502 microprocessor and one 40 pin wire wrap socket. The microprocessor plugs into the wire wrap socket. This assembly plugs into the main logic pcb in place of the 6502. The pins 26-33 on the bottom of the wire wrap socket are cut short so they do not reach the pins in the socket on the main pcb. The pins 26-33 are wired under the wire wrap socket to +5V and Gnd to force a hex EA on the microprocessors data bus.

THEORY:

The hex EA instruction for the 6502 is a NOP (no operation). When the 6502 reads the NOP instruction it does no operation except increment the program counter and read the next instruction another NOP. This forces the microprocessor to count through all the 65536 possible addresses on its 16 bit address bus. If the address bus lines are monitored on a scope AB0 will be a square wave clocking with a 2uS period, AB1 4uS, AB2 8uS, AB3 16uS, AB4 32uS and so on. Each higher address line having twice the period of the one before. This gives a predictable set of signals to trace.

OPERATION:

Insert the NOP wire wrap socket into the 6502 socket on the main logic pcb. Apply power. Scope buffered address lines on the PET memory expansion connector. Start at BA0 and move up through BA11. Check for a square wave at each with equal amplitude and a period of twice that of the last address line.

PROBLEMS:

If there are no signals on the address lines then the uP may not be running. Check for +5V on pin 8 of the 6502. Switch the PET on & of to assure a rest. The IRQ (pin 4) and RES (pin 40) should remain high. A 1uS clock signal should come in on pin 37 and out on pin 39. If the 6502 is reading the NOP's then a 2uS square wave should be on the SYNC line (pin 7) of the 6502. (Pins 9-25) If these are not working , the address buffers may not be working. Check the power supply regulators on the main logic pcb.

Any odd, non square wave signal could be caused by a short to another signal line. Follow the bad address line back to its buffer, scope lines which run parallel. Look for a signal which has the same shape as the bad address line.

PROBLEMS Cont:

If a short is found use an ohmmeter with a low scale (> 20 ohms) to probe toward the real short.

Any buffered address line stuck in a hi or low condition could indicate one of two failures:

1) A short to +5V or GND respectively. Use of a low ohmmeter between the address line and +5V or GND should locate it.

2) A bad buffer chip. Check the signal into the related buffer chip, if it is good and the output is not shorted or without supply then the buffer is bad.

A stuck low signal could also be caused by an open track. The open can be found by scoping back towards the address buffer for that stuck line.

6502 Microprocessor Signals

uP pin #	FUNC	uP signal
9	AB0	2uS
10	AB1	4uS
11	AB2	8uS
12	AB3	16uS
13	AB4	32uS
14	AB5	64uS
15	AB6	0.128mS
16	AB7	0.256mS
17	AB8	0.512mS
18	AB9	1.024mS
19	AB10	2.048mS
20	AB11	4.096mS
22	AB12	8.192mS
23	AB13	16.384mS
24	AB14	32.768mS
25	AB15	65.536mS
4	Not IRQ	Hi
6	Not NMI	Hi
7	SYNC	2uS
34	R/W	Hi
39	Theta 2	1uS
40	Not RES	Hi

J9 Edge Connector Signals

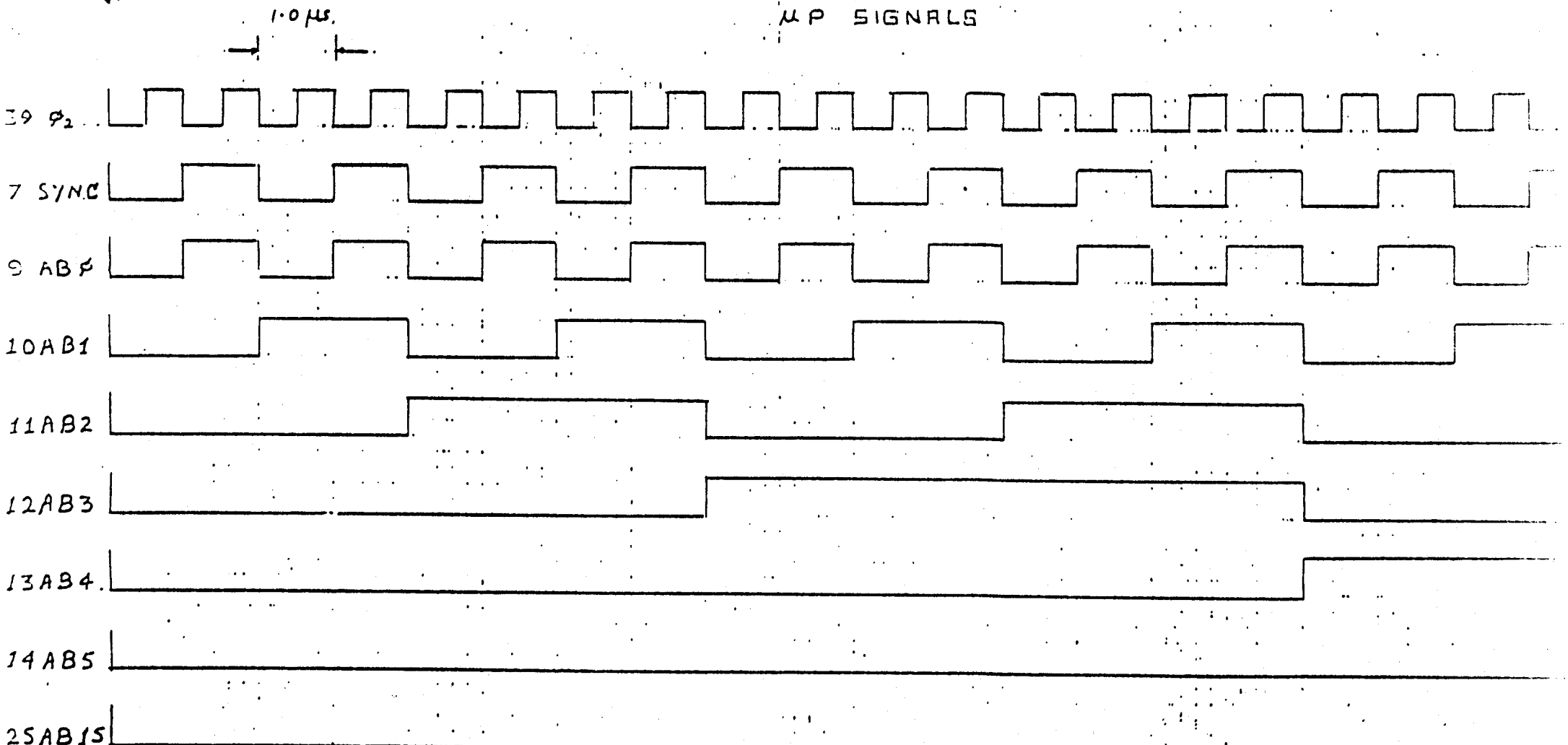
Edge conn Pin #	FUNC	Edge Conn Signal
A2	BA0	2uS
A3	BA1	4uS
A4	BA2	8uS
A5	BA3	16uS
A6	BA4	32uS
A7	BA5	64uS
A8	BA6	0.128mS
A9	BA7	0.256mS
A10	BA8	0.512mS
A11	BA9	1.024mS
A12	BA10	2.048mS
A13	BA11	4.096mS
A14	BA12	8.192mS
A15	BA13	16.384mS
A16	BA14	32.768mS
A17	BA15	65.536mS
A18	SYNC	2uS
A21	B Theta 2	1uS
A22	BR/W	66mS Hi/4.15mS Low
A23	Not BR/W	66mS Low/4.15mS Hi

J4 Edge Connector Signals

Edge Conn Pin #	FUNC	Edge Conn Signal
A10	Not SEL2	66mS Hi/4.15mS Low
A11	Not SEL3	"
A12	Not SEL4	"
A13	Not SEL5	"
A14	Not SEL6	"
A15	Not SEL7	"
A16	Not SEL8	"
A17	Not SEL9	"
A18	Not SELA	"
A19	Not SELB	"
A22	Not RES	Hi
A24	Not NMI	Hi

PET NOP TESTER

μP SIGNALS

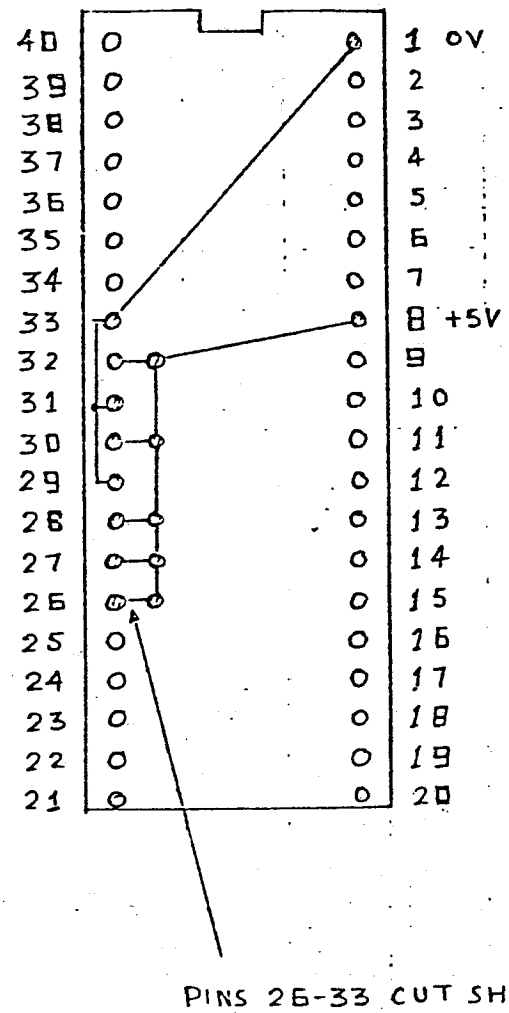


PET NOP TESTER

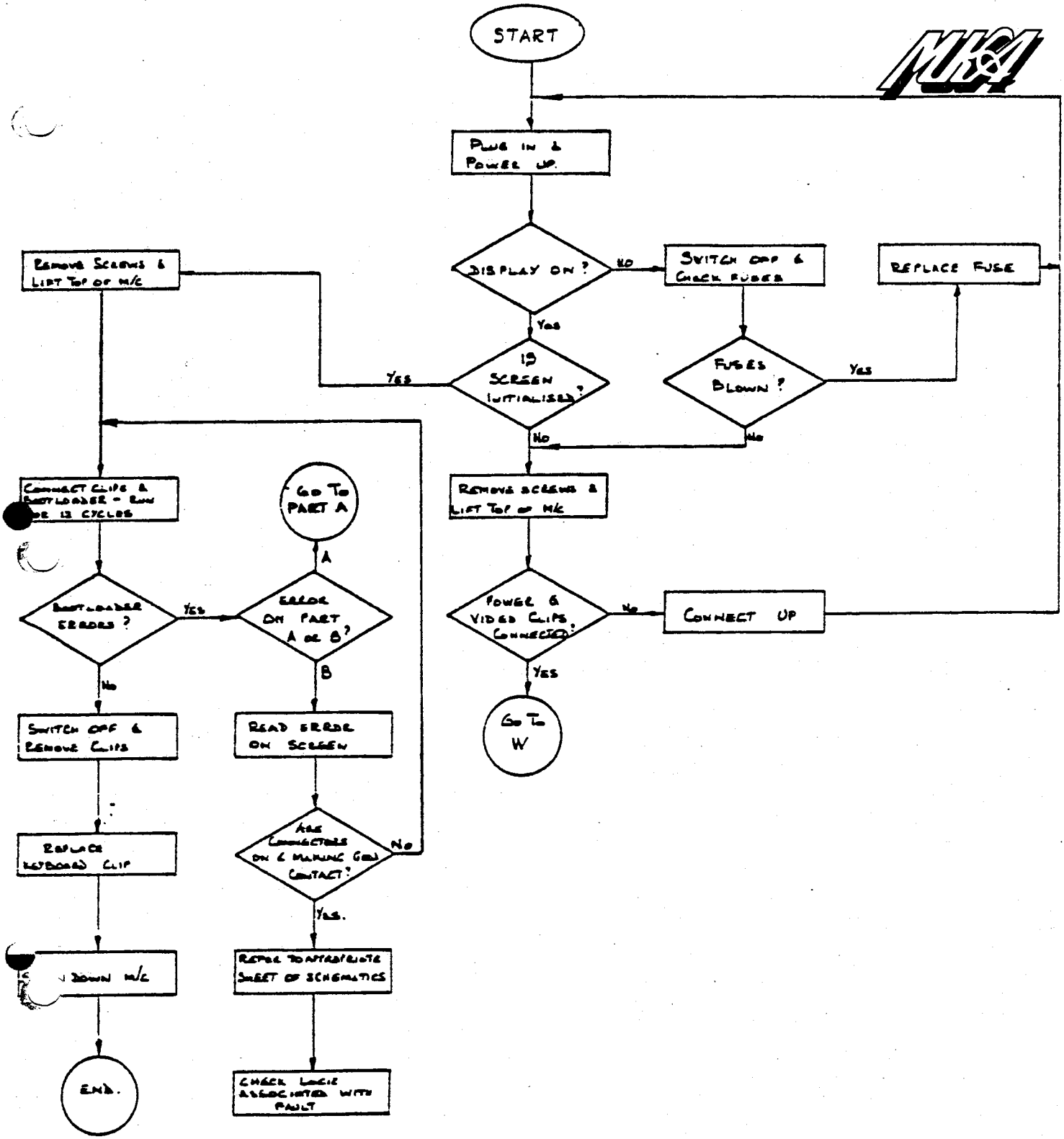
6502
TOP VIEW

VSS	1	40	$\overline{RES}$
RDY	2	39	ϕ_2
ϕ_1	3	38	SO
IRQ	4	37	ϕ_0
NC	5	36	NC
NMI	6	35	NC
SYNC	7	34	R/W
VCC	8	33	DB0
AB0	9	32	DB1
AB1	10	31	DB2
AB2	11	30	DB3
AB3	12	29	DB4
AB4	13	28	DB5
AB5	14	27	DB6
AB6	15	26	DB7
AB7	16	25	AB15
AB8	17	24	AB14
AB9	18	23	AB13
AB10	19	22	AB12
AB11	20	21	VSS

WIRE WRAP SOCKET
BOTTOM VIEW

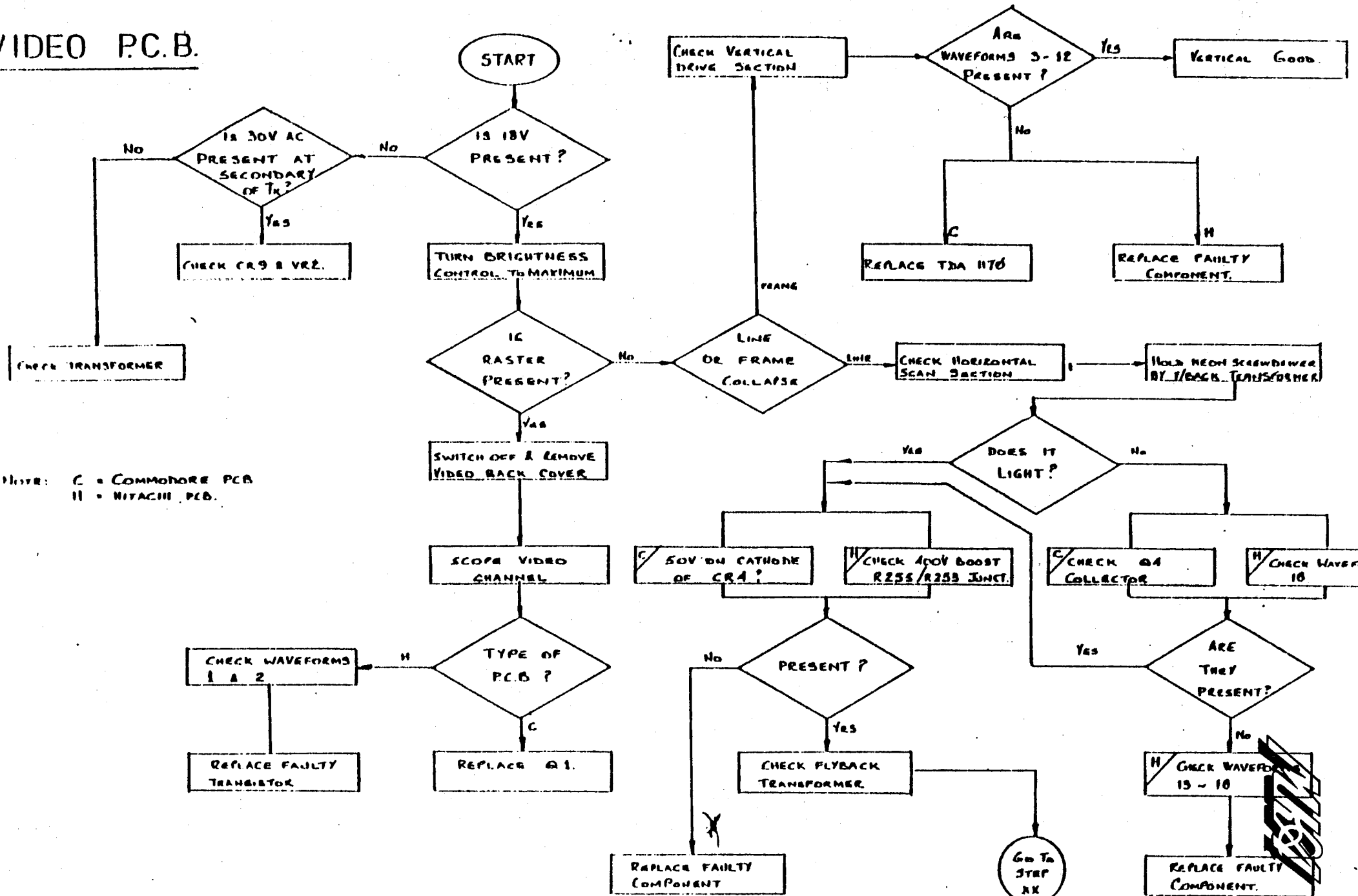


FORCES 6502 TO A NO OP (EA) CAUSING ADDRESS BUS TO COUNT UP IN BINARY ALLOWING OSCILLOSCOPE TO BE USED TO CHECK ADDRESS BUS



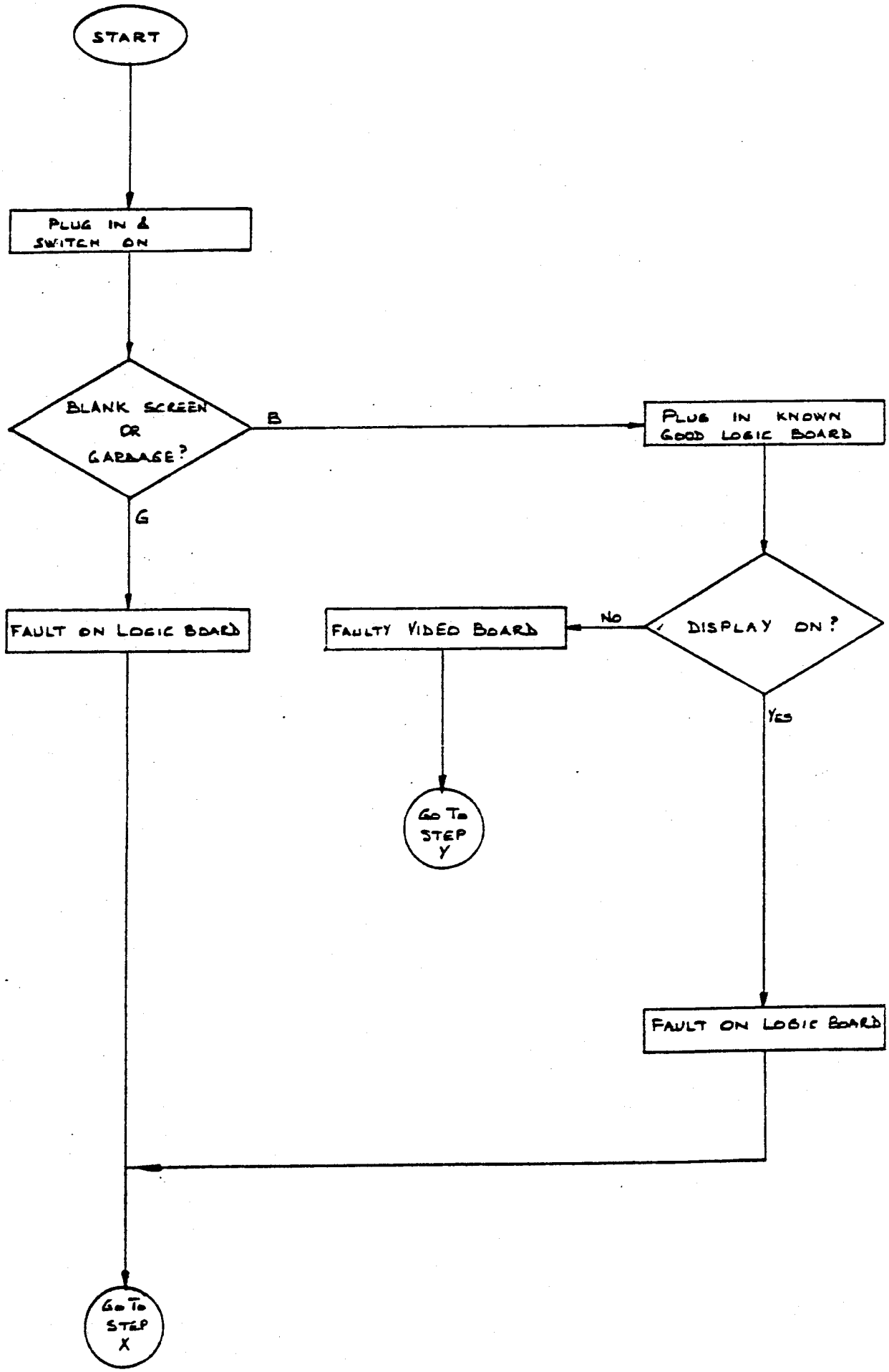
PET FLOWCHART

VIDEO P.C.B.



Note: C = Commodore PCB
H = Hitachi PCB.

STEP W


START
PLUG IN & SWITCH ON
BLANK SCREEN OR GARBAGE?
B
G
PLUG IN KNOWN GOOD LOGIC BOARD
DISPLAY ON?
NO
YES
FAULTY VIDEO BOARD
FAULT ON LOGIC BOARD
FAULT ON LOGIC BOARD
GO TO STEP Y
GO TO STEP X

STEP X

1. CHECK D.C. SUPPLY RAILS
   (a) + 5v DC Junction of CR7 & C11
   (b) + 5v DC Junction of CR6 & C9
   (c) + 12v DC Junction of CR5 & C7
   (d) - 5v DC Pin 1 of any MAIN RAM

2. CLOCK (Pins 37,39) on 6502

3. CHECK RESET line (Pin 40)
   Should be high

4. GO TO STEP Y

STEP Y

There are two different types of boards:
   (a) Commodore (green pcb) C (Ref 8032033/34)
   (b) Hitachi (yellow pcb) H (Ref 321448/49)

They are divided into 4 sections:
   (a) Line output (horizontal scan)
   (b) Frame output (vertical scan)
   (c) Video (amplified & fed to CRTC cathode).
   (d) Power supply (common to the 3 sections above)

NOTE: Always check for 18v

IMPORTANT: When troubleshooting video pcb, look for waveforms on pins 3, 5 and 7 of video connector. If no signal is present on any of these test points, then unplug video connector and scope the corresponding pins on J7 logic pcb.

STEP XX (IMPORTANT: CARE MUST BE TAKEN DURING THIS STAGE AS THERE IS VERY HIGH VOLTAGE PRESENT WHICH COULD PROVE FATAL IN EXTREME CASES)

1. SWITCH OFF
2. Unclip EHT connector from tube
3. Grip connector by cable in INSULATED pliers
4. Hold long screwdrivers blade half an inch from cables metal "fork" pins
5. Switch on.
6. If spark is strong and bright, then switch off, reconnect and check all connections to CRT.
7. If no spark, then Flyback transformer faulty.

NOTE: EXTREME CARE MUST BE TAKEN IF THE CRT TUBE IS REPLACED AS THERE IS DANGER OF IMPLOSION IF CARELESSLY HANDLED. INDUSTRIAL SAFETY GOGGLES MUST BE WORN AT ALL TIMES. NEVER HANDLE THE TUBE BY THE NECK AS THIS IS THE WEAKEST PART.

LOADING VIC PROGRAMS ON PET

To load programs written on VICS to run on PET use the following POKES before the first load:

From 5K VIC:	POKE 4096,0 POKE 41,16
From 8K VIC:	No change
From 13/21/27.5K VIC:	POKE 4608,0 POKE 41,18

Tranfers from PET to VIC need no changes.

Alternate method is to type:

REM.....

On PET:

Load VIC program

POKE 1025,2

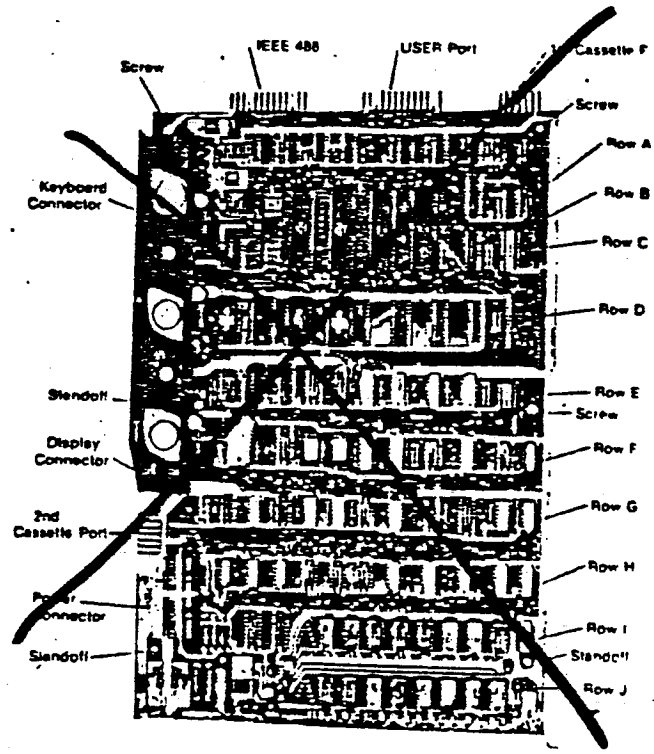
For 5K VIC:	POKE 1026,16
For 13/21/2705K VIC:	1026,18

NOTE: For 8K VIC: No change just load

Then remove line 0 like 50.

This method forces the VIC program to start at 1024, the previous method forces the PET to start at where the program is wasting memory.

Using the alternate method the VIC program should not have a line 0.



C. Test

The Diagnostic Fixture consists of a 40-pin clip, to which is attached a small box containing a 2716 EPROM, a 74LS138 gate chip, a RESET pushbutton, and an LED.

The test fixture is clipped onto the 6502 CPU. The keyboard and User Port Diagnostic Jumpers in place. Turn on power switch.

The test fixture LED will light, indicating that there is + volts on the board and that the test fixture is correctly clipped onto the 6502.

Upon pressing the RESET button, the 6502 will attempt to address the ROM in the FXXX address range; the fixture will force this address to be 9XXX, to execute the program in the test fixture ROM.

The operator will monitor the test results via message on the CRT, as described below.

The second test also executes from the Diagnostic Test Fixture ROM. This is not a full test of the dynamic RAM but simply verifies that the RAM (Z page and stack) may be written and read, and that the program may proceed to the next test. If this is not successful, the program will stay in a loop, attempting to write and read the failing RAM address. The operator may then use the scope to check the RAM address, data, and control signal as required.

Upon successful completion of the first tests, the ROM will write the remaining tests from itself into dynamic RAM, and jump to the RAM to execute them. They will then proceed as described below:

TEST SEQUENCE FOR DIAGNOSTIC CLIP

1.0 Test screen
2.0 Test Z-page
3.0 Test stack
4.0 Move diag. prgm.
5.0 Wait for clip to be removed
6.0 Checksum ROM 8D (EØØØ)
7.0 Check IRQ vector ROM 9D (FØØØ)
8.0 Count down before INIT
9.0 INIT all I/O, CLR screen
10.0 Time 60 Hz IRQ
11.0 Horz. Drive Test
12.0 Test Dyn RAM
13.0 Checksum all 5 ROMs (CØ-FØ)
14.0 Test keyboard
15.0 Test timers (5C-6522)
16.0 Test Cass #1 and Cass #2 IRQ's
17.0 Test IEEE-488 DIO BUS
18.0 Test IEEE-488 Control BUS
19.0 Beep, Pass message and # of cycles check for loop switch.

1.0 Test Screen

a) Write pattern into screen. Read and test pattern.
b) Indicate defective TV RAM chip or address line.

2.0 Test Z-Page

a) Zero stack page for later test
b) Fill Z-page with pattern and test the pattern
c) Indicate defective I.C. or address line.

3.0 Test Stack

a) Check stack still zero, indicate any address failure
b) Fill stack with pattern and test the pattern
c) Indicate defective I.C. or address line

4.0 Move Diagnostic Program

a) Copy 8 pages from Boot ROM into Dyn RAM
b) Test moved copy
c) Indicate defective I.C. or address line.

5.0 Wait for Clip to be Removed

a) Blink "Remove Clip" message
b) Check Reset vector for clip removed
c) Debounce clip removal.
d) Determine Dyn Ram size (16K or 32K)

6.0 Checksum ROM 8D ($E000-$E7FF)

a) Perform 3 byte checksum of ROM of E000 to E7FF
b) Indicate defective I.C.

7.0 Check IRQ Vector ROM 9D (FØØØ)

a) Test locations $FFFE and $FFFF for correct data.
b) Indicate defective I.C.

8.0 Count down before INIT

a) Time delay for operator to read screen.

9.0 INIT all I/O

a) Call INIT routine in operating system.
b) Test video for full blank screen.
c) Test 60 Hz IRQ

10.0 Time 60 Hz IRQ

a) Compare 1 60 Hz IRQ to register counters.

11.0 Horz. Drive Test

a) Window low and hi side of Horz. Drive signa

12.0 Test Dynamic RAM

a) Fill all Dynamic RAM with test pattern
b) Test pattern
c) Indicate defective I.C. or address line

13.0 Checksum all ROMs

a) Perform 3 byte checksum on all 4 ROMs
b) Indicate defective I.C.

14.0 Test Keyboard

a) Drive each column, read each row
b) Toggle defective line

15.0 Test Timers

a) Compare 6522 timers to reg counters
b) Cause IRQ's from timers.

16.0 Test Cassettes

a) Cause IRQ for each cassette.
b) Check for correct IRQ

17.0 Test IEEE-488 DIO Bus

a) Write all 256 combinations out IEEE-488 DIC
b) Read verify each
c) Toggle defective lines

18.0 Test IEEE-488 Control Bus

a) Toggle each line separately
b) Read verify each
c) Toggle defective line.

19.0 Blink PASS MESSAGE

a) Blink Message
b) Test PIN-E USER Port for Loop Diag. Functi

D. Results:

1. As each test starts, it will be identified on the TV screen. If t PCB passes all tests the message "PASS CYC ØØØØØØ" will be displayed. Diagnostic Program will th loop through the tests.

2. If any failure occurs, it will be displayed on the TV scree and chip failures will display the column and row on t logic PCB.

Additional Features:

1. Repeat Test
   a) Failure in RAM and ROM tests automatically repeat test pattern on address and data lines.
   b) I/O test failures will toggle the bad I/O line.
2. Repeat all tests
   a) Automatic Repeat after "PASS CYCLE ØØØØØ(message.

E. Software

The first three tests in the Diagnostic are executed solely fro the ROM on the Diagnostic Test Fixture. Successful completic of the first test indicates that the 6502 can fetch and execu instructions and that, in general, the CPU's address data, an control busses are okay. This is indicated by the CRT display (the sign-on message. The Diagnostic Program will then pro ceed to the second test.

ITEMS	LOCATION	QUANTITY
BASIC 4.0 ROMs		
901465-22	UD6	
901474-04 (01)	UD7	
901465-21	UD8	1 set
901465-20	UD9	
901465-23	UD10	
DOS 2.1 (4040)		
901468-12	UL1	
901468-11	UJ1	1 set
901468-13	UH1	
901466-04	UK3	
DOS 2.5 (8050)		
901482-07	UL3	
901482-06	UH1	1 set
901483-04	UK3	
DOS 2.6/7 (2031)		
901484-05	U5F	
901484-03	U5H	1 set
IC's		
6500		1
6522		2
6532		2
6561		1
6502		1
6504		1
RAMs		
2114 DISK DRIVE -		2
4116 PET CBM.		
PRINTER ROMs		
325301-01 (4022)	U8D (Bi-directional)	1
325320-01 (8022/3)		1
MISCELLANEOUS		
901527-02 (7805) 5V Regulator		1
901527-04 (7818) 18V Regulator		1
LEDs (Green 903811-03, Red 990082)		2

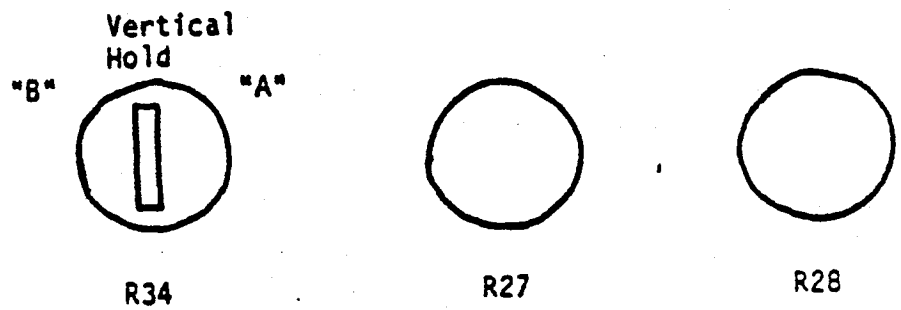
VERTICAL HOLD ADJUSTMENT PROCEDURE
FOR 80 COLUMN PETS

1. Rotate vertical hold pot (R34) on video board fully clockwise. (see figure below)

2. Rotate vertical hold pot clockwise until picture locks. Note position of wiper of pot "A".

3. Continue rotating counter-clockwise until picture starts to roll upward. Note new position of wiper of pot "B".

4. Back off pot by clockwise rotation to point halfway between "A" and "B".



SIGNAL FORMAT ON CBM CASSETTES

1. Explanation of CBM Recording Scheme

The CBM cassette deck uses an unequalised constant current recording method to place data on magnetic tape. The encoding scheme uses three distinct full cycle pulses. (See Figure 1). The data zero or one is represented by a pairing (or dipole) of a short and a long pulse. If the long pulse is first, the dipole is one, if the short is first, the dipole is zero. The byte mark occurs once each byte and provides a reference for byte identification.

2. CBM Playback Circuit.

The CBM cassette playback circuitry first amplifies the recorded signal then passes this through equalisation and squaring circuits. Thus a logic-level signal is presented to the computer. The computer measures the time between the negative edges of the signal and decodes the data from these measurements.

3. Points to Note

a) The CBM computer outputs data during WRITE to the cassette with the information carried in the **positive** going transitions and accepts data during READ with the information carried by the **negative** going edges. (See Figure 2).

b) Because of this encoding scheme the data is polarity sensitive. A 180 deg. phase reversal to proper data produces unreadable data. To check for proper data polarity with an oscilliscope, connect the scope to the READ data line from the cassette to the computer. Put the tape to be checked into the cassette and press PLAY. Set the horizontal rate to 100uS/cm and the triggering for negative going edges. Set the vertical scale to 1V/division and center the wave form on the screen. Adjust the scope trigger so that the displayed waveform is at the center of the left edge of the screen. The signal should appear as shown in Figure 3, with the negative going edges of the short and long pulse clearly visible. Depending on the scope used and the data, the byte mark negative edges may also be visible.

Try switching the polarity of the scope trigger to positive going edges and observe if the positive edges are closer to the proper timing than the negative edges. If the positive edges are better, then the recorded data has the wrong polarity.

c) Because of the high frequency emphasis encountered with audio cassette recording the phase of the signal may shift as much as 90 deg. This produces read data which is halfway toward being reverse polarity. This situation is evident when the scope shows negative and positive edges to be equally far from the proper timing. A partial phase shift (much less than 90 deg.) usually accompanies tape duplication, and this is visible on the scope as a widening of the negative going edges. Generally, better duplication has been obtained with the high frequency peaking in the duplicator master deck reduced to nearly minimum.

d) The level at which a CBM cassette deck records is around 500 nanowebers per meter (nWb/m), which is just under saturation on low coercivity tapes. It has been found that duplicated tapes perform better when their level is slightly higher than the CBM tape level. It is also possible to fully saturate the tape and obtain good duplication results. Generally then, the rule on recording level is 'The higher, the better' provided the duplicating equipment can handle these elevated levels.

e) The CBM data is recorded 1/2 track on 1/8 inch tape. It has been found that when the data is duplicated with some stereo heads, the head skew and differing phase relationship between the 2 tracks causes a distorted signal and reduced readability. It is therefore best to use monoaural heads on duplicator slaves which are to be used for duplicating CBM tapes.

FIGURE 1:
DATA TIMING

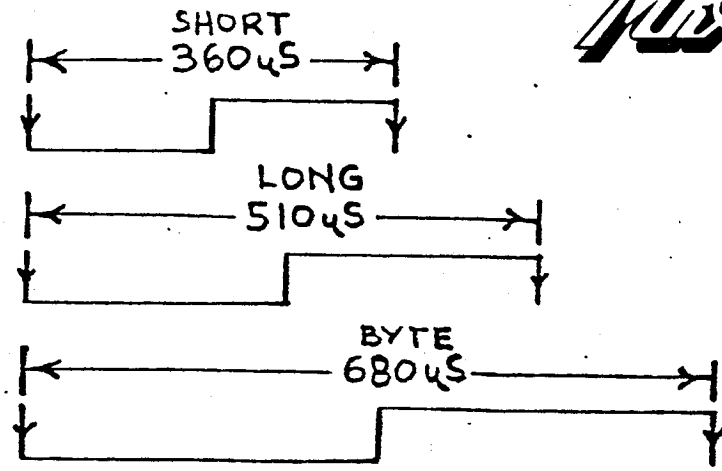


FIGURE 2: DATA IN/OUT

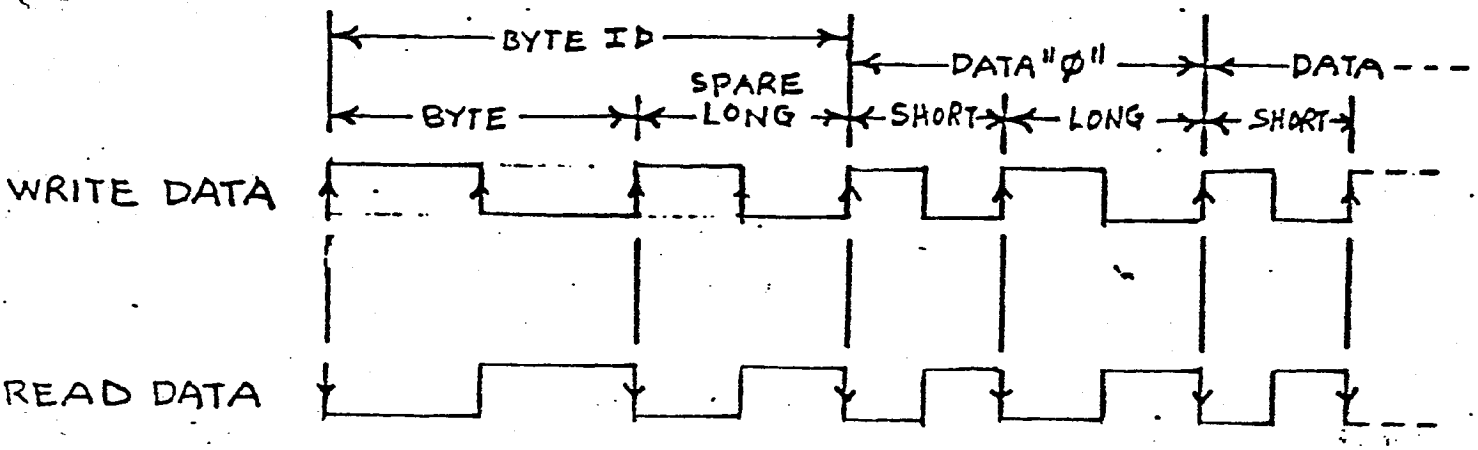
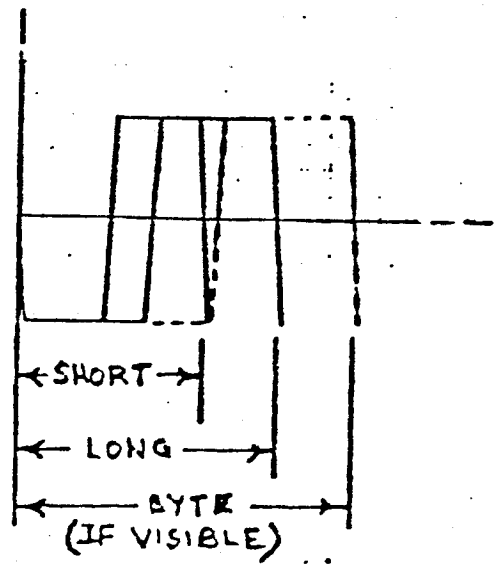
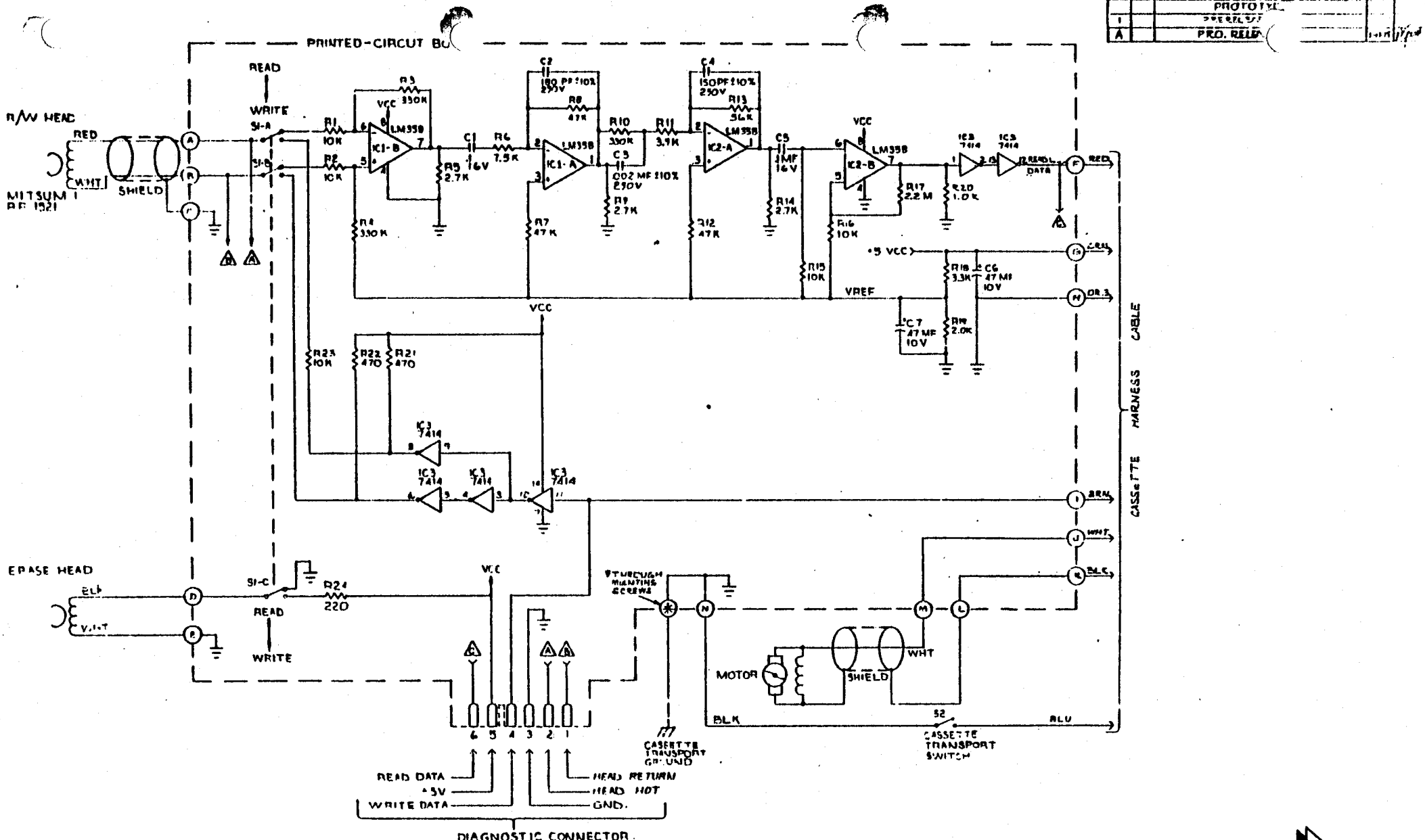


FIGURE 3:
READ DATA
SCOPE DISPLAY





LAST USED	NOT USED
R24	
C7	
S2	
IC3	

ALL RESISTANCE VALUES ARE IN OHMS, 1/4W ±5%.
NOTES: UNLESS OTHERWISE SPECIFIED —

commodore

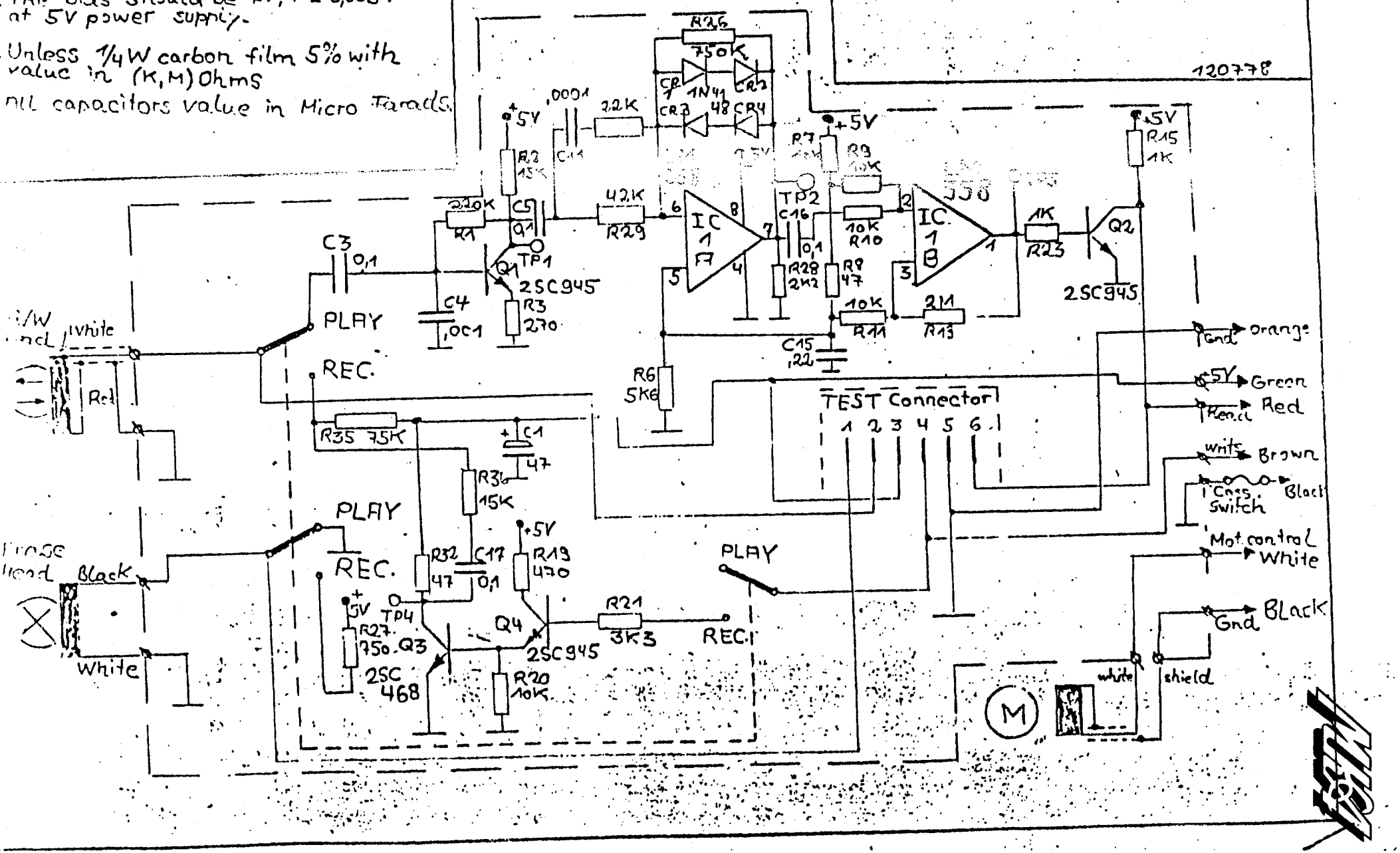
SCHEMATIC DIAGRAM
CASSETTE

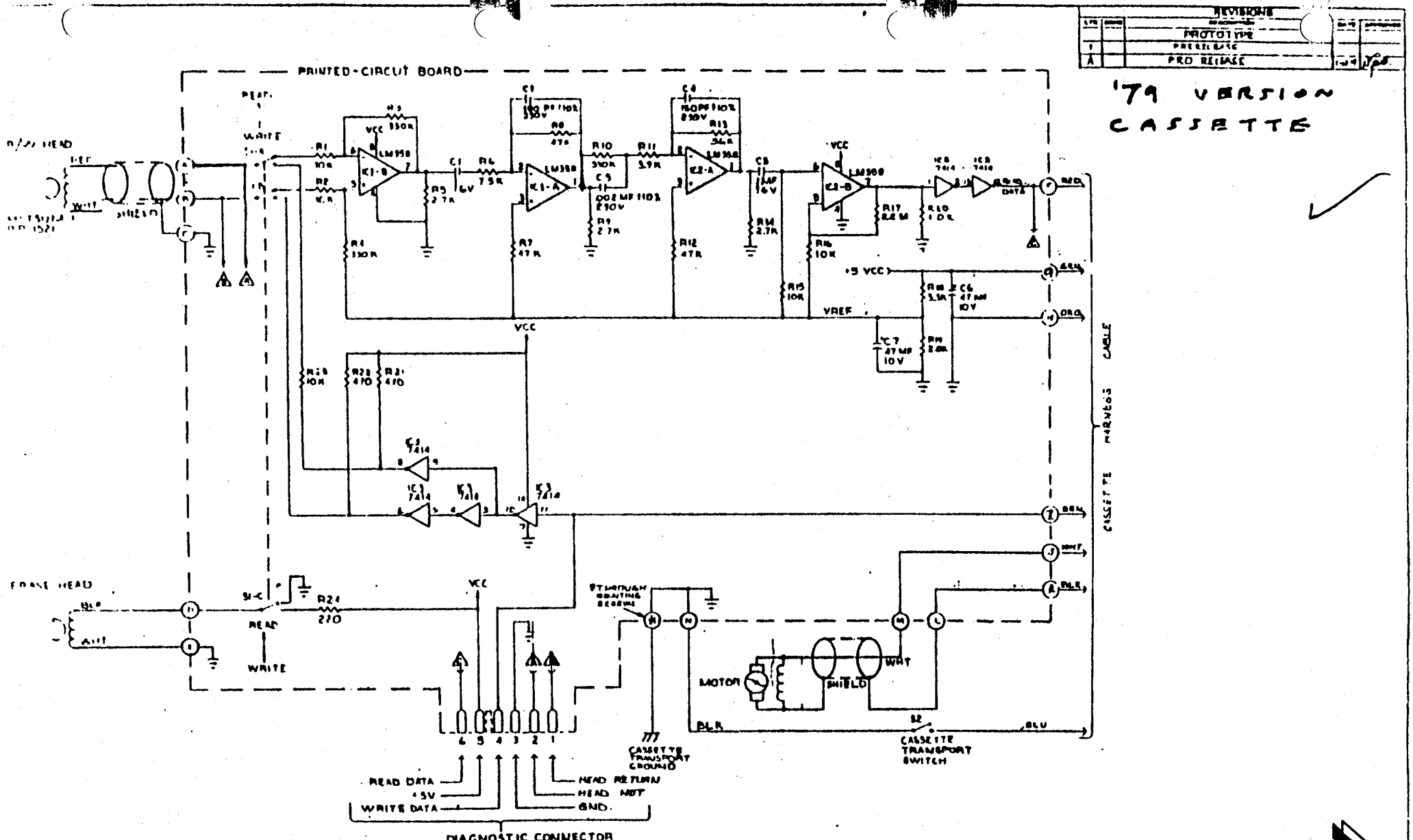
326274

Notes: 1. R6, R7, R8; ±2% 1/4W
2. The bias should be +1,7 ±0,005V at 5V power supply.
3. Unless 1/4W carbon film 5% with value in (K,M) Ohms
4. All capacitors value in Micro Farads.

Commodore "datasette"

120778





'79 VERSION CASSETTE

REVISIONS			
LTR			
		PROTOTYPE	
A		PRE-RELEASE	
		PRO RELEASE	

ALL RESISTANCE VALUES ARE IN OHMS, 1/4 WATT 5%.
NOTES: UNLESS OTHERWISE SPECIFIED

LAST USED	NOT USED
U14	
C8	
R24	
IC5	

SCHEMATIC DIAGRAM PET-CASSETTE

320

Table 17. User's Quick Reference—Disk Commands

BASIC 3.0	UNIVERSAL DOS SUPPORT	BASIC 4.0
SAVE "dr:fn",8	SAVE"dr:fn",8	DSAVE,"fn",Ddr (drive defaults to 0)
LOAD"dr:fn",8	/dr:fn (searches both drives)	DLOAD"fn",Ddr (drive defaults to 0)
LOAD"*",8 RUN	↑dr:fn	DLOAD"fn",Ddr RUN
LOAD"dr:fn",8	↑*	shifted RUN/STOP
LOAD"$0",8 LIST (destroys memory)	>$0 (preserves memory)	DIRECTORY or DI<shifted R> (preserves memory)
10 OPEN1,8,15 20 INPUT#1,A,B$,C,D 30 PRINT A,B$,C,D	> return	?DS$ or ?DS (DS is number of error only)

NOTE: Assume that OPEN1,8,15 has already been typed for all of the PRINT# commands in the following formats. Commands may be spelled out or abbreviated by the first letter as illustrated.

	INITLIALIZE	
PRINT#1,"Ix"	>Ix	PRINT#1,"Ix"
	VALIDATE	
PRINT#1,"Vdr"	>Vdr	COLLECT Ddr
	SCRATCH	
PRINT#1,"Sdr:fn"	>dr:fn	SCRATCH"fn",Ddr
	DUPLICATE	
PRINT#1,"Dddr=sdr"	>Dddr=sdr	BACKUP Dsdr TO Dddr
	COPY (all disk)	
PRINT#1,"Cddr=sdr"	>Cddr=sdr	COPY Dsdr TO Dddr
	COPY (single file)	
PRINT#1,"Cdr:dfn= dr:sfn"	>Cdr:dfn=dr:sfn	COPY Ddr,"sfn" TO Ddr,"dfn"
	CONCATENATE FILES	
PRINT#1,"Cdr:dfn= dr:sfn1,dr:sfn2,...	>Cdr:dfn=dr:sfl, dr:sfn2,...	CONCAT Ddr,"sfn" TO Ddr,"dfn"
	RENAME FILES	
PRINT#1,"Rdr:dfn=sfn"	>Rdr:dfn=sfn"	RENAME Ddr,"sfn" TO "dfn"
	FORMAT A DISKETTE	
PRINT#1,"Ndr:dname,xx"	>Ndr:dname,xx	HEADER "dname",Ddr,Ixx