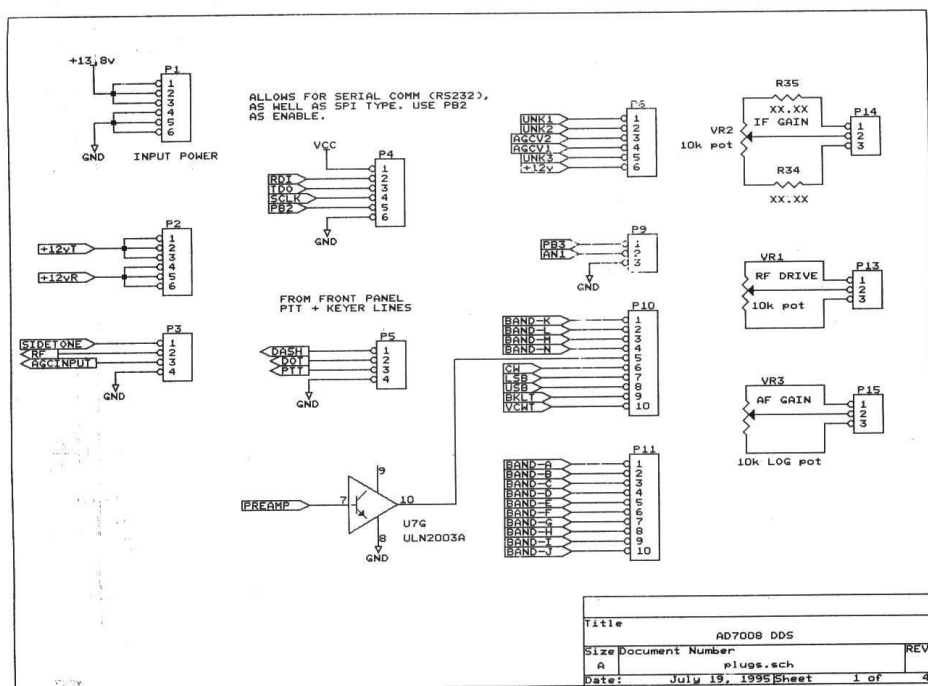
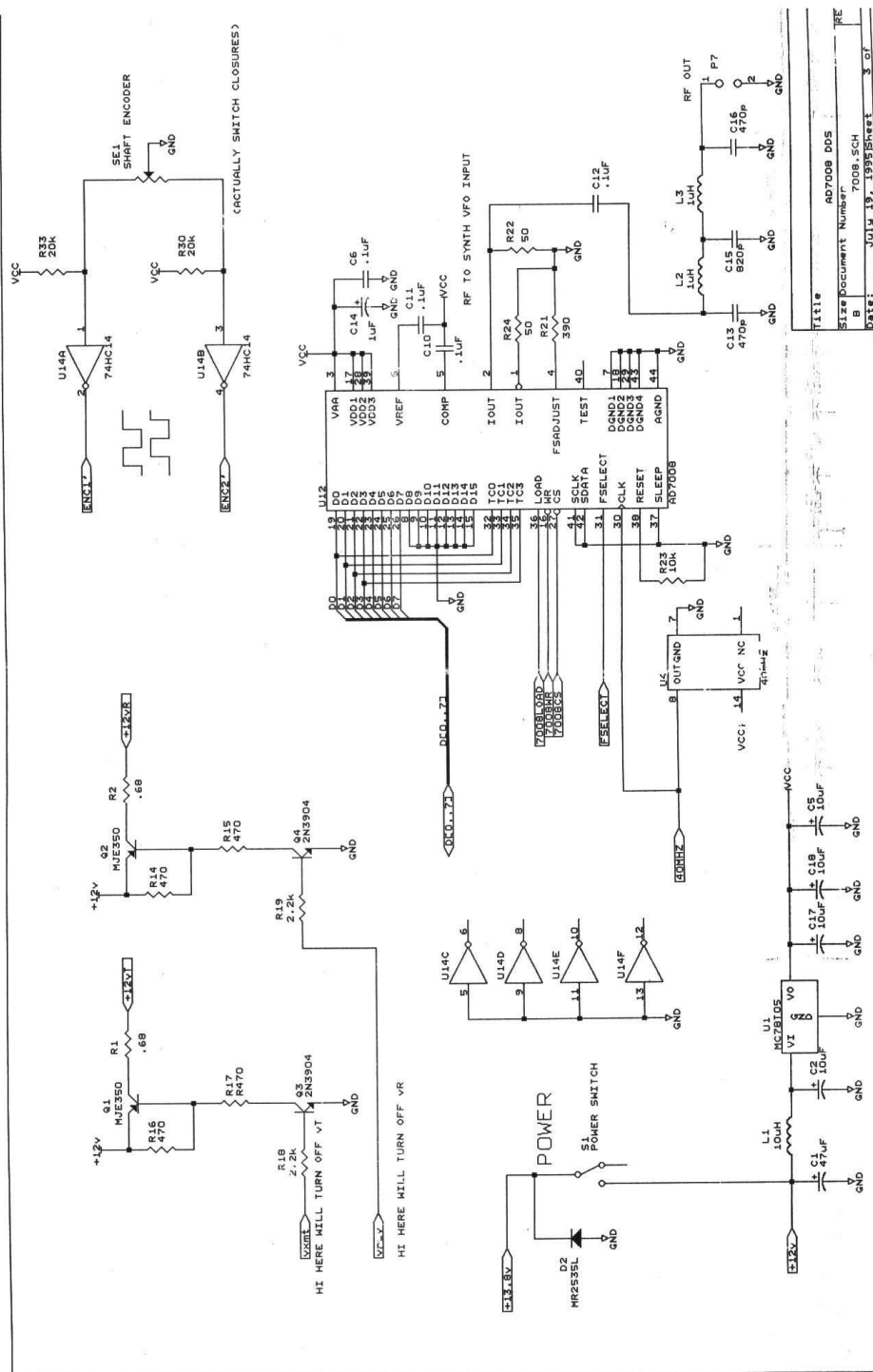
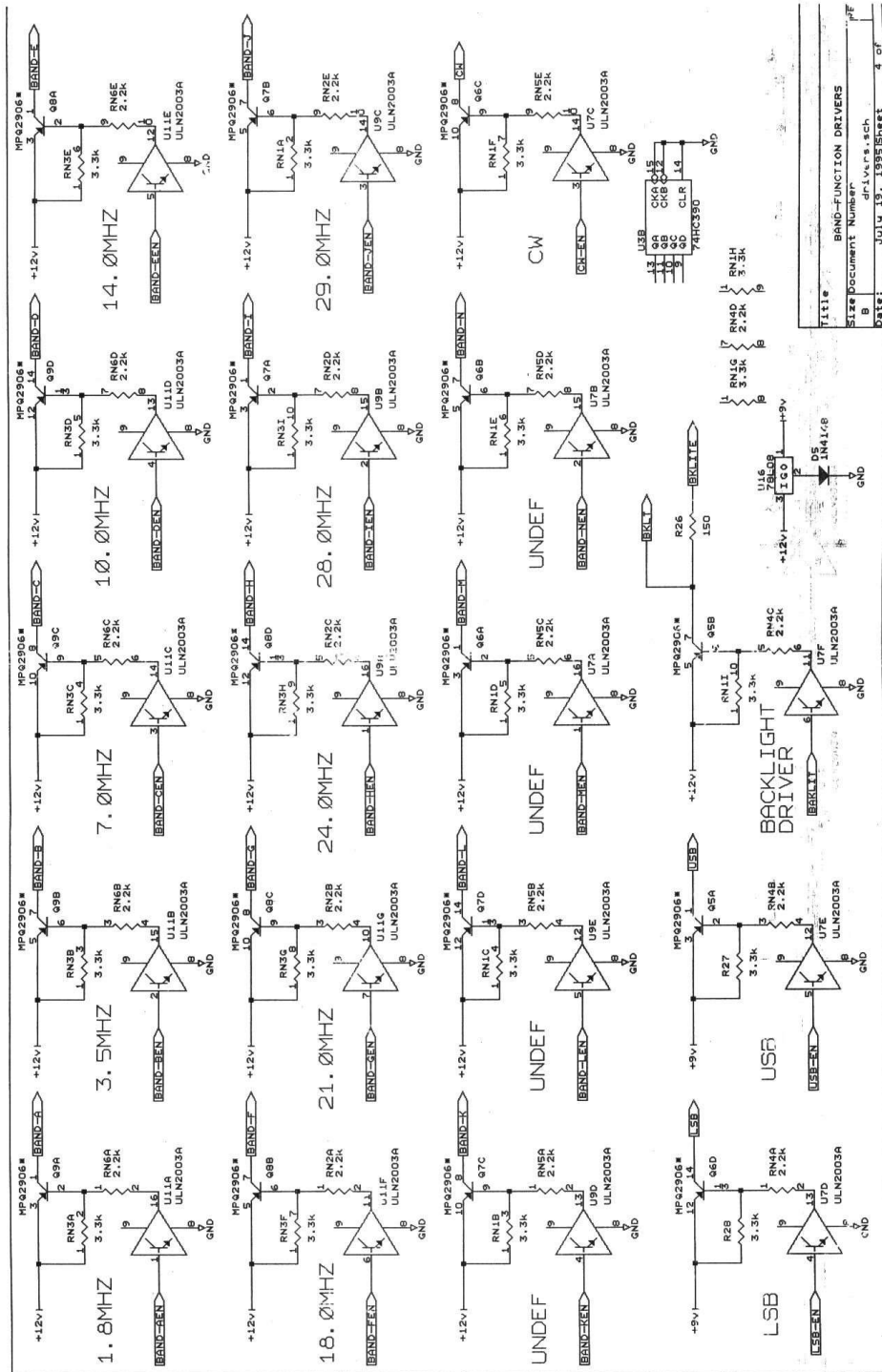


PARTS LIST

R1,2	0.68R	Q5,6,7,8,9	MPQ2N906 or EP2015CN
R3,4,5,6,7,8,9		ABOVE IS DIL ARRAY	
10,12,20,23,25,31	10K	U1	MC78T05 or LM340T5
R11,27,28	3K3	U2	MC68HC705B5FN
R13 1K R14,15,16,17,32	470R	U3	74HC390
R18,19	2K2	U4	40MHZ DIL OSC
R21	390R	U5	93C56
R22,24	51R	U7,9,11	ULN2003A
R26	150R	U6,8,10	74HC595
R29	300R	U12	AD7008JP50
R30,33	20K	U13	74HC164
R34,35	NOT INSTALLED	U14	74HC14
RN1,3 [PIN1 COMMON]	3K3	U15	MC3406
RN2,4,5,6 [ISOLATED]	2K2	U16	78L08
VR1-5	10K	LCD1	16chr X2line
C1 47uF			
C2,5,7,17,18	10uF TANT		
C3,14	1uF TANT		
C4,6,8,9,10,11,12,19,20	100N [104]		
C13,16	470PF [471K]		
C15	820PF [821K]		
D1,3,4,5	1N4148		
D2	MR2535L /1N5408		
Q1,2	MJE350		
Q3,4	2N3904		

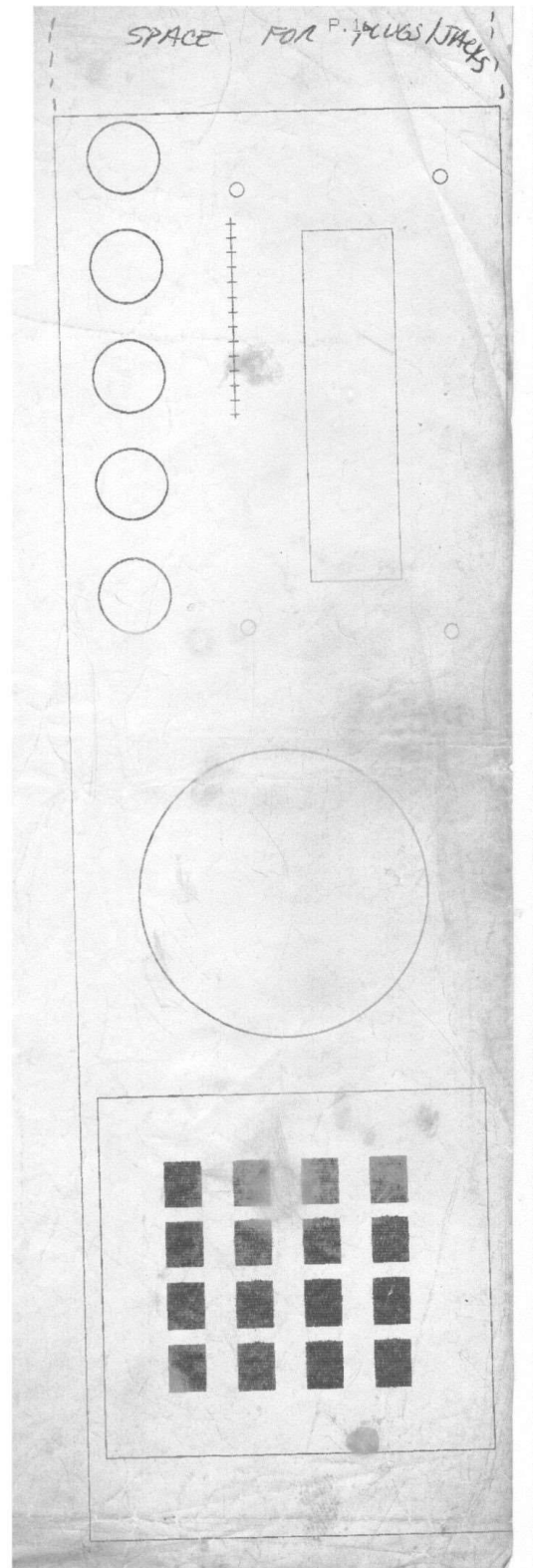






MAR 01 '95 11:51AM MCU APPS

TO: SHELDON HANDS
8 PAGES



SPECIFICATIONS:

1. DRILL FROM TOP SIDE.
2. HOLE DIAMETERS ARE AFTER PLATING.
3. ALL DIMENSIONS ARE IN INCHES AND ARE $\pm .010$ UNLESS NOTED.
4. ALL HOLES TO BE PLATED THRU UNLESS OTHERWISE NOTED.

MATERIAL:

1. BOARD THICKNESS: .062 INCHES.
2. FRA

FINISH:

1. 2 OUNCE COPPER.
2. SOLDER COAT.

DESIGN RULES

MINIMUM TRACK WIDTH	13
PAD TO PAD CLEARANCE	13
PAD TO TRACK CLEARANCE	13
TRACK TO TRACK CLEARANCE	13

LAYER: SDR6 GREEN

NOTE: ALL LAYERS OF THIS ARTWORK ARE VIEWED FROM THE TOP SIDE

AERO ELECTRONICS	
PROJECT: RTX DOS/MCU	
SCHEMATIC REVISION: 1	P08 REVISION: A
SCHEMATIC FORMAT: Omsd	DATE: 2/28/95
P08 LAYOUT FORMAT: Tmgo	

SYMBOL	DRILL SIZE + .003 / - .003	QUANTITY (PLATED)
+	.028	82
X	.038	277
Y	.046	18
T	.073	6
Z	.125	9
M	.140	1

