TESLA MH74S571 Editor xB6 bytes

4Mhz clock - 1 µcycle = 1µS

```
C40F  INIT
36
C400              P2  ->  RAM
32
C400              initialise address
CA0C
CA0E
C478              't' for TESLA
CA08
C401               P3H  ->  SCIOS
37
9023               JMP  NOBLOW
C43F  DISPLAY
33                 P3  ->  DISPD-1
3F                 wait for keypress     ! uses P1 !
9006             *command*   JMP  ADROK
C41A             *hex*
33                 P3  ->  ADR-1
3F                 new address for display  ! uses P1 !
900F               JMP  TRUNCATE
E403  ADROK
9817               = TERM  ->  BLOW
40
E423
9C06               = GO  ->  NOBLOW
AA0C
9C02               MEM + 1
AA0E
C20E  TRUNCATE
D401
CA0E               address <x200
C400  NOBLOW
CA12               MASK set 00 -  just read
901C               JMP  DOIO
C449  BLOW
CA02               Zap-flag into display
C43F
33                 P3  ->  DISPD-1
3F                 wait for keypress     ! uses P1 !
9005             *command*   JMP  CHKBLOW
40               *hex*
CA0D                new 4 bits into display
90F1               JMP BLOW
C400  CHKBLOW
CA02                clear Zap-flag
40
E422
9CE2               = MEM or TERM   ->  NOBLOW
C408
CA12                MASK set 08 – zap and read
C40E  DOIO
35
C400               P1  ->  IO
31
C4FF               both Ports all output
C922
C923
C20C  POWERUP
C920               ADL to Port A
C212               MASK
9C1D               not zero  ->  BLOWBITS
C20E  READBITS
DC20                ADH  with  PB5
C921  _ _ _ _ _     to Port B                  >  5V on  <
C4E1
C923               bits 4-1 Port B set to input
C91F  _________    PB7 on              >  output enable  <
C121               read 4 bits   ~35µS
C90F  _________    PB7 off                    >  o/e end  <
1C
D40F               isolate 4 bits
CA0D               into display
C400
C921  _ _ _ _ _  _ all outputs off             >  5V off  <
C920
908C               JMP  DISPLAY
D20D  BLOWBITS     use MASK to select bit
01
40                 align for Port B
70
DC20               include PB5
DA0E               and ADH
C921  _ _ _ _ _     to Port B                  >  5V on  <
C458      [t5]      ~30µS
C91E  _ _ _ _ _     PB6 on                     >  10V on  <
8F00    [t3 + t1]   200µS
C91F  _________     PB7 on                     >  o/e on  <
C4E3      [X]       1mS
8F01                *zap 1 bit*
C90F  _________     PB7 off                    >  o/e end  <
C458      [t2]      ~30µS
C90E  _ _ _ _ _     PB6 off                    >  10V off  <
8F00    [t4 + t5]   200µS
C400
C921  _ _ _ _ _     all outputs off            >  5V off  <
C920
C212
1C                  shift MASK – next bit
CA12
90AF               JMP POWERUP
DB
```

[tn] see **TESLA** timing diagram