ELECTRONICS TOMORROW

by John Miller-Kirkpatrick

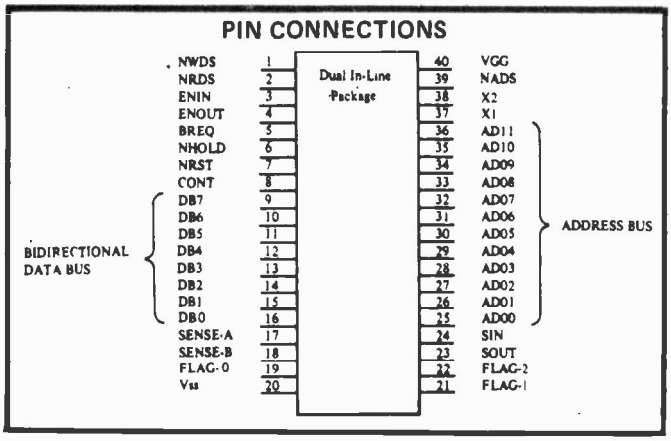
WHAT A SCAMP!

National Semiconductors have been in the MPU market for some time with their PACE and IMP systems which are both designed for use in major computer sized machines. Now they have introduced SC/MP in the smaller MPU market, an 8 bit CPU in a single 40 pin package at a low price and with the usual NS technological back-up. SC/MP is intended for use in general-purpose applications where the cost per function is the most important factor as SC/MP is slower than the F8 and 6800 CPUs. For most applications the speed is not an important factor as the MPU is used to replace TTL type logic circuitry which would be too complex to build or require too much power for the required function. SC/MP includes a variety of useful functions that are not even provided by other MPU systems, like self-contained timing circuitry, 16 bit (65K) addressing capability, serial or parallel data transfer and common memory/peripheral instructions. These built-in features are combined with the low unit-cost make SC/MP the ideal answer to many applications which could not previously have been considered.

All input and output pins are TTL compatible and are also TRI-STATE which means that in addition to logic '0' and Logic '1' there is a third state of the outputs where the output will follow the status of any other TRI-STATE output connected in parallel with the first without t amage to either output driver. This is similar to Wire ORing TTL outputs using the open collector gates except that in the latter a logic '1' on either (or any) parallel output will produce a logic '1' on the wire ORed line, with the TRI-STATE outputs the output is in a high impedance state until it is enabled thus one may choose logically which of the paralleled outputs is to be enabled and put data onto the common bus.

IN-OUT or IN-OUT

The 40 pin pin-out of the SC/MP CPU chip is shown as fig 1. The functions of these pins working from pin 1 are as follows.



NWDS is an output to indicatae to peripherals that CPU data is now valid, ie WRITE.

NRDS is an input which allows data from the data bus into the CPU, ie READ.

ENIN, ENOUT, BREQ are controls used in multiple CPU systems to denote which CPU chip has access to the address and data busses.

NHOLD this input causes the I/O address and data busses to lock in their present state until NHOLD input goes high, this can be used for slow I/O devices such as humans.

NRST reset input, when this is set low or on CPU power-on the internal registers are all initialised and the program pointer points at location Hex 0001.

CONT this input is similar to NHOLD except that the CPU is halted before fetching the next instruction whereas NHOLD stops it halfway through an instruction.

DB 0-7 Parallel I/O bus to/from ROMs, RAMS, I/O units, etc.

SENSE-A this is an external interupt signal which can be sampled by the CPU or can be used to cause immediate transfer to an interupt program, and is usually used by I/O devices to indicate that they wish to access the CPU.

SENSE-B this input is similar to SENSE-A except that it will not cause immediate transfer to another program as it has to be sampled by the CPU program. It could be used with SENSE-A to indicate a particular type of interupt.

FLAG 0-2 These are output indicators to indicate to other units user designated states of the CPU or other peripherals. For instance they could be used as acknowledgment indicators in peripheral handshake routines to indicate to the peripheral that its interrupt request has been noticed by the CPU.

SIN, SOUT are serial I/O pins. An instruction will cause a data bit at SIN to be transferred to an internal register or from the register to SOUT, this is used for example in teletype I/O or other VDU, CASSETTE, or KEYBD I/O routines.

ADAO-11 This is a 12 bit address bus which can directly access any location within a 4K 'page' it can be used in conjunction with the data bus to access any location within the 65K maximum for the CPU.

X1-X2 These are the timing pins which can have a 1MHz crystal on a 500pF capacitor connected across them, the crystal is only used where accuracy of instruction times is required, ie if an accurate DELAY is required.

NADS This is one of the most important pins on the whole device, its basic function is to denote to any I/O or memory unit that a valid address is available on