Circuit Ideas

Simple tester for f.e.ts

Zero-bias drain current, gate cut-off voltage and gate leakage current in junction f.e.ts can be measured with a high-impedance voltmeter (20,000 Ω/V or better) using the circuits shown in figures (a), (b) and (c) respectively. Using an external voltmeter, a simple tester can be built around three push-button switches as shown (right). With the source resistor value of 1k Ω, I_{DDS} is read in mA on the voltage scales of the meter. Two small 9-V batteries give sufficient voltage to test most f.e.ts. The f.e.t. is protected by the protection circuit (2N1711) which works on the loadline principle, and limits the power to the test circuit to about 200mW.

The circuit has an additional refinement. By depressing the V_P button and the I_{DSS} button simultaneously, the circuit shown in (d) is made. The meter reading now gives both drain current in mA and gate-source voltage in volts, thus giving a third point on the $I_D V_{GS}$ characteristic.

The complete tester can be built in a box measuring 10 × 7 × 5cm.

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