Integrated Vacuum Microelectronics

Brian P. Otis
EECS 243
May 2002

INTRODUCTION

The practice of using controlled electron propagation in a vacuum to achieve signal gain has been around since the patenting of the triode vacuum tube in 1907 [1]. Although vacuum electronics enabled early radio, television, and computing, they have disappeared in all but a few specialty applications such as high-power RF transmission and certain military systems. Integrated solid-state devices have taken over as a versatile, cheap, and robust alternative to vacuum electronics. This paper examines the potential for a new generation of vacuum electronics. Similar to modern solid-state systems, these devices would be integrated and micro-scale in nature. It will be shown that there are definite advantages to vacuum electronics in certain solid-state dominated applications, as well as sizable challenges that must be surmounted before the technology is successful. The fabrication of these devices will be explored, and the achievable device performance will be evaluated. Finally, future work to advance the field will be proposed based on the findings of the paper.

STATEMENT OF PROBLEM

The transistor was a Nobel-prize winning discovery that redefined the system of use of active devices in electronics and enabled systems that were previously impossible to realize. The state-of-the-art in solid-state electronics allows high frequency operation, low power consumption, low cost, and high fabrication yield. However, there are certain applications where solid-state devices are impractical or inconvenient, and one potential solution is the same vacuum technology that was abandoned nearly 50 years ago.

Radiation Stability

There are extreme applications that render traditional solid-state devices useless due to their inherent sensitivity to harsh environments. For example, the sensing electronics in nuclear and fusion reactors are subjected to high levels of radiation. Electronics in space are also inherently subjected to high levels of radiation. This radiation can generate charge carriers in the bulk of solid-state devices. This can cause transient artifacts in the operation of the device (soft errors) and, in some cases, permanent damage (hard errors).

Current Solution: Rad-Hard ICs

One obvious solution to this problem is to use a radiation shielding material, such as Aluminum or Carbon [2]. A more elegant solution is to use radiation hard (rad-hard) fabrication techniques to enable solid-state devices to withstand these high temperatures. One way of doing this is hardening the oxide layer, making the device less susceptible to radiation damage. Another option is to use silicon-on-insulator (SOI) substrates, which have been shown to reduce radiation-induced failures. These methods also require very conservative (and inefficient) circuit design to take into account the maximum predicted radiation damage (i.e., threshold voltage shifts due to radiation damage). A more brute-force approach is to use built-in self testing (BIST) and redundancy to mitigate the failures due to radiation. This method increases the complexity and power consumption of any given system, and doesn't actually address the problem of radiation damage.

Potential Solution: Vacuum Electronics

Unlike solid-state devices that use a single crystalline active channel, vacuum electronics utilize a vacuum channel. Thus, it is not possible to induce carrier generation through radiation [3]. Therefore, vacuum electronics are relatively immune to radiation damage, making them suitable for the aforementioned high radiation environments.

High Temperature Stability

Other crucial applications, such as aircraft and machine sensing applications, require high temperature operation. For example, aircraft engine sensors must be placed on engine surfaces, necessitating a high operating temperature [4]. Similarly, the field of bore-hole profiling (and many other heavy machinery applications) requires instruments placed at high temperatures locations to sense various equipment functionality [3].

Current Solution: Remote Electronics or Custom ICs

Currently, high temperature sensing requires the electronics to be placed in a shielded location away from the sensor. This necessitates long wires between the sensor and electronics, reducing the efficiency and accuracy of the system. Fuel cooling is sometimes used in aerospace to cool these electronics [4]. It has been estimated that if high-temperature stable electronics could be used on an F-16 fighter, the result would be a savings in hundreds of pounds of weight and millions of dollars in savings per aircraft [4]. To this end, custom silicon-carbide (SiC) integrated circuits have been pursued. Devices using this substrate have been shown to have a higher temperature tolerance than silicon-based devices.

Potential Solution: Vacuum Electronics

Vacuum devices are inherently tolerant to high temperatures. Similar to a vacuum device's inherent immunity to radiation, their vacuum channel is not susceptible to

thermal induced carrier generation [3]. This gives vacuum electronics the potential for higher temperature stability than silicon and SiC based devices. Immunity to high temperature allows closer placement to high temperature measurements and a reduced need for heat transfer accessories (heat sinks, etc) for power electronics. Indeed, macro-scale vacuum electronics are still popular in the high-power RF transmission community for this very reason.

STATE OF THE ART

To date, there has been substantial work in the field of integrated vacuum electronics. Even after vacuum electronics witnessed their end in popularity in consumer goods, researchers tried to build ever-smaller vacuum devices for the applications mentioned above. With the advent of reliable thin-film and bulk microfabrication, new opportunities emerged for vacuum electronics researchers.

Vacuum Electronics Introduction

Vacuum electronics can be broadly separated into two categories: Thermionic emission or Field emission. The difference concerns the way electrons are emitted from the cathode. In both cases, the emitted electrons are accelerated towards the anode's high potential through a vacuum channel. The path of the electrons is affected by modulating the voltage on a grid electrode placed between the cathode and anode. Thus, signal gain can be achieved. Multiple grids can be placed between the cathode and anode, as shown in the conceptual drawing below.

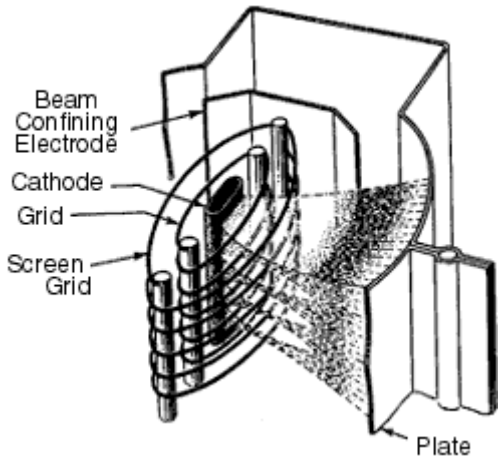

Figure 1. Beam Tetrode [5]

These additional grids can shape the I-V characteristics of the device, increasing the output resistance and decreasing the feedthrough capacitance of the device. Next, this paper describes the two types of electron emission categories.

Thermionic Emission

Thermionic emission relies on a heated electron emitter, or cathode. The cathode is heated up enough such that the electrons receive enough kinetic energy to leave the

surface of the cathode. Thermionic devices display the obvious disadvantage that a heating element is needed in every device. Depending on the cathode material used, a temperature of at least 1000K is needed to induce electron emission. However, as shown in the next section of the paper, these devices can be relatively easy to fabricate using traditional IC fabrication techniques.

Field Emission

Field emission, unlike thermionic emission, is possible with a *cold* cathode. Despite the obvious advantage of not requiring a heating element, the fabrication of these devices presents multiple problems. The field emission is highly dependent upon the size and work function of the emitter. Small emitter sizes are achievable through modified IC fabrication processes, and the cold cathode is appealing from a power efficiency standpoint. Because of this, field emission is often seen as the preferred integrated solution. Field emission is possible when an electric field above approximately 0.5V/Å is placed on a metal surface in a vacuum chamber [6]. To achieve uniform field emission with reasonable anode voltages, it is necessary to use a needle-shaped emitter with a tip radius less than about 1μm [6]. Reducing this radius further provides additional field enhancement, allowing a lower anode voltage that increases the usefulness of the device. Thus, although a cold cathode is desirable from a system-level standpoint, fabrication difficulties are encountered in the quest to increase the sharpness of these tips. Indeed, much work has focused on reliable and reproducible fabrication of sharp emitter structures. Currently, stable currents of approximately 10μA per tip can be obtained. Arrays of these tips can be used to obtain higher current drive capabilities.

In general, there are two types of integrated field emission tips: vertical and lateral. As shown in Figure 2 below, vertical devices need special fabrication techniques to make the tip, but the anode, grid, and insulating material is very similar to traditional IC fabrication.

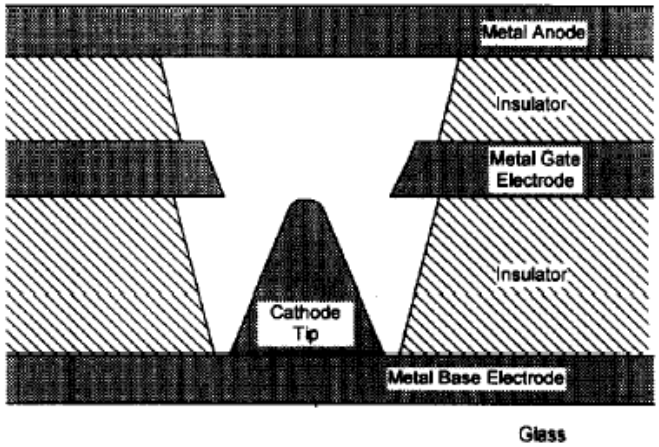

Figure 2. Vertical Field-Emission Triode [6]

Lateral devices, on the other hand, attempt to form a sharp tip using 2D lithography techniques from above, and occasionally specialized etching to further sharpen the tip. See Figure 3 below.

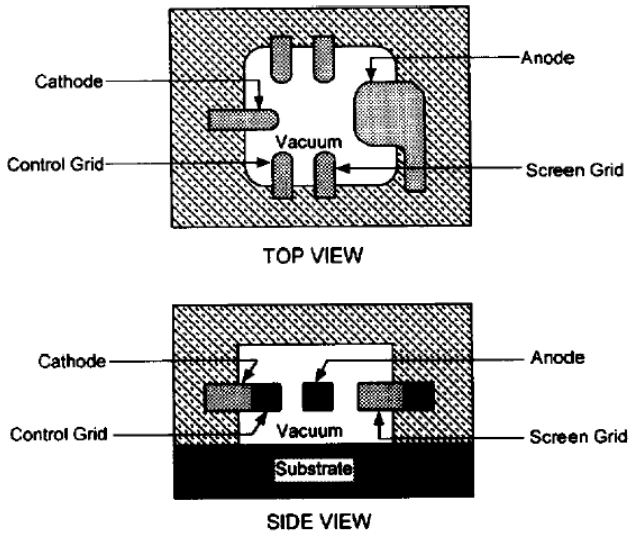

Figure 3. Lateral Field-Emission Triode [6]

All micro-scale field emission devices suffer from fast current fluctuation, causing very noisy device operation [6]. Though not well understood, this noise source has been measured to be over five orders of magnitude above the shot noise and could prove to be problematic for sensitive applications. Another issue with field emission devices is their lifetime. Sputtering of the tip by ionized residual gasses has been shown to decrease the tip lifetime and degrade device performance.

CRITICAL REVIEW OF CURRENT WORK

In order to plan future research directions to meet the aforementioned applications of integrated vacuum electronics, it is important to review current techniques and identify relevant features and shortcomings. This section critiques the state-of-the-art in integrated vacuum microelectronics, and the final section proposes future work on the subject.

Thermionic Devices

As previously stated, most integrated vacuum device research has been done with a field emission philosophy. However, thermionic excitation should be reviewed, as it lifts some of the fabrication constraints placed by the creation of field emission tips. This topology will be evaluated for its fabrication feasibility as well as its performance potential.

One planar thermionic structure, as shown below in Figure 4, has been fabricated and tested [7].

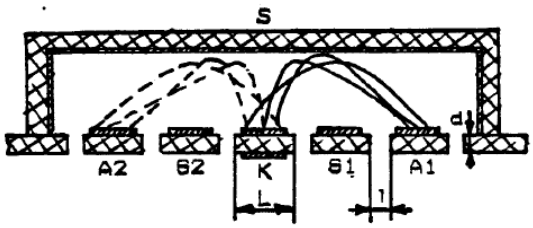

Figure 4. Integrated Lateral Thermionic Triode [7]

In this device, a localized cathode heater is used to induce electron emission. The width of the electrodes is approximately 100μm, and the spacing between electrodes is 10μm. Using this device, an integrated, functioning relaxation oscillator has been built. The necessary anode voltage was 50V. To heat the emitter, 30mW was dissipated in the integrated cathode heater. The fabrication of this device is extremely simple, relying on evaporated thin films. Slots are etched into the substrate to confine heating to the cathode electrode.

There are potential problems with this strategy that could prevent large-scale use. First, as shown in the figure above, the devices are very large. The packing density would be low, and would be unappealing from a system-level point of view. It is possible to scale the dimensions down, but the current drive capability would decrease accordingly. From a fabrication standpoint, it would be difficult to define submicron electrodes since deep etching is required to thermally isolate the cathode from the other electrodes. From a performance perspective, large planar structures such as this one suffer from high parasitic capacitances, reducing the bandwidth of the device. Although vacuum devices have a very fast transit time (the speed of an electron in a vacuum device is usually more than 2 orders of magnitude higher than the speed of an electron in a silicon substrate, approximately 10^7 cm/s) [3], the device is fundamentally limited by the ratio of its transconductance to its input capacitance. Thus, this device will have bandwidth constraints that remain constant with the scaling of device size.

However, with this topology, the ease of implementation is very intriguing. Traditional IC fabrication techniques can be leveraged, and it may be possible to decrease the parasitic capacitances with the thick, low-K dielectric that the IC industry is already pursuing. Most importantly, a functioning, integrated circuit has been demonstrated, providing a proof of concept that has been somewhat elusive in integrated vacuum microelectronics.

Field Emission Devices

The second class of vacuum electronics uses field emission. This type of emission has excited device engineers for decades because of the promise of high current densities, low power consumptions, and the possibility of fabricating very sharp tips to allow field enhancement, thus allowing low anode voltages. Additionally, vacuum electronics using field emission could leverage years of work

on making sharp, integrated field emission tips for displays. This section critiques these works and discusses the usefulness of these devices.

As mentioned earlier in the paper, lateral emission devices are promising because they can potentially allow sharp tip formation using standard IC fabrication techniques. One recent effort attempted to exploit this opportunity as well as perform in-situ vacuum encapsulation of the device [8]. As shown in the following top view of the device, a sharp 2D tip was defined using traditional lithography techniques.

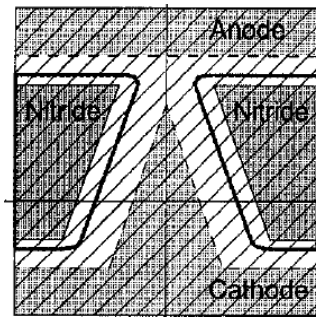

Figure 5. Top View of Lateral Vacuum Device [8]

The structure was formed by the following simplified process flow:

1. LPCVD thick nitride
2. Deposit 500Å buffer oxide
3. Deposit 1000Å N^+ poly
4. Deposit 500Å buffer oxide
5. Deposit 5000Å nitride
6. Deposit 3000Å thick oxide
7. Layers etched via RIE with PR mask
8. Poly over-etch with SF_6 to form cavity
9. Thermal oxidation to sharpen tip (O_2, 120min, 1000^{o}C)
10. Wet etch to evacuate cavity
11. E-beam evaporation of molybdenum to seal chamber (0.1μTorr)

The clever part of this design was defining a 2D tip using optical lithography and forming a 3D tip by utilizing the silicon consumption of thermal oxidation. The following cross section is the result of the above process flow.

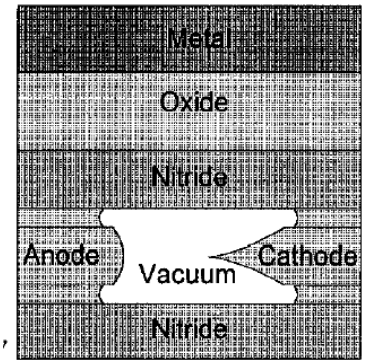

Figure 6. Cross-Sectional View of Lateral Vacuum Device [8]

The tip-sharpening mechanism uses a LOCOS-like process, and the result is basically an inverted bird's beak.

Since the device has an integrated vacuum chamber, it was tested in an ambient pressure environment. The measured performance indicated a current density of 2μA/tip at an anode voltage of 30V. The low anode voltage required proves that a sharp tip was fabricated, thus increasing the usability of the device. Using an array of emitters could easily increase the current drive capability of the device. As previously mentioned, the bandwidth of a vacuum device is limited by its transconductance (g_m) to input capacitance ratio. The measured g_m of this triode was 1.7μS. This g_m would require a parasitic capacitance of less than 3fF to obtain a usable bandwidth of 100MHz. It would be difficult to obtain a capacitance less than this, so the bandwidth of this structure is limited by its low g_m. Using an array of emitters would linearly increase the g_m, but would also linearly increase the capacitance, keeping the bandwidth constant.

In summary, this lateral emitter approach displays the benefits of having a cold cathode (no heater), a low required anode voltage, and in-situ vacuum encapsulation. Though not as straightforward as the planar thermionic vacuum device, the fabrication of the lateral field emitter does leverage current IC fabrication technologies. One issue with this design is the packing density of arrays. Since the structure is lateral, the number of tips per area is less than with a vertical emitter structure. Another issue is that the absolute anode to cathode spacing is dependent upon the thermal oxidation of the poly cathode. This dependency would inherently cause mismatches in the cathode to anode spacing, and hence mismatches in the turn-on voltage of these devices. This mismatch would make realistic circuit design difficult and inefficient. One final problem with this design is that the high temperature thermal oxidation sharpening step necessitates a large thermal budget.

Another recent design utilizes an IC fabrication phenomenon that is generally considered undesirable to achieve sharp emitters [9]. As shown in Figure 7 below, "nanopillars" were formed on a tungsten surface to form the emission tips.

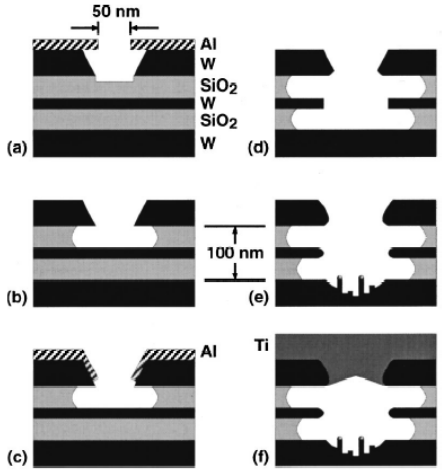

Figure 7. Vertical emitters using self-aligned RIE [9]

The first part of the process flow, as shown in the above figure, is fairly straightforward. However, after the cavity is formed, AuPd is deposited onto the tungsten, resulting in grain nucleation of about 2.5nm. This nucleation is the heart of this process flow. These grains act as a "self-aligned" RIE mask for the emitters. An RIE is performed (CF_4, O_2), which etches the unprotected tungsten and reduces the AuPd grain size to about 1nm. The result is tungsten pillars with a radius on the order of 1nm and a height of up to 10nm (Part e. in the figure above). An angled evaporation of Ti was used to encapsulate the structure at about 0.75μTorr.

The measured performance of the device shows a current drive of up to 10nA at an anode voltage of 15V and a transconductance (g_m) of up to 6nS. It has been shown that, although there are multiple field emission tips in each structure, the field emission is dominated by the single tip with the highest electric field [9].

This design represents a large departure from standard IC fabrication techniques. By using non-traditional methods, very small tips were produced and the entire device occupied less than a few hundred square nm. The current drive and g_m are very low, but this design is conducive to large arrays that would increase the drive capability. High bandwidth circuits are unlikely, however, as the intrinsic g_m is very low. Indeed, it would even be difficult to achieve DC signal gain with a transconductance this low. Thus, the g_m of the device must be increased before system implementation is practical.

One potential problematic area in this design is the reliance on accurate grain nucleation for the critical device dimension. Nucleation sites that are larger than anticipated would lead to large pillars (small electric fields and high turn-on voltages). Smaller than anticipated sites would be completely etched away, leaving short (or completely missing) pillars. Since an arrayed device would most likely be necessary anyway, redundancy would be added that could potentially offset this problem. It is interesting to notice that none of the fabrication steps involve extremely high temperature processing. This characteristic will be investigated in more detail at the end of the paper.

The final example of a vertical field-emission vacuum device uses directional wet etching of (100) silicon to produce a pyramidal emitter tip [3]. A cross section of the device is shown below in Figure 8.

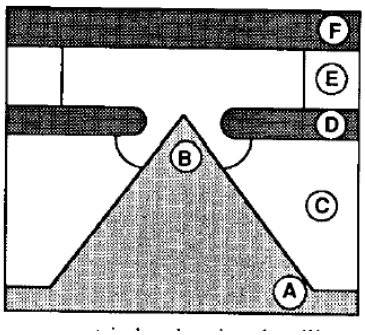

Figure 8. Vertical emitter via directional wet etch of Silicon [3]

The emitter (labeled A in the figure above) is etched out of the silicon substrate. A rectangular nitride mask is used to promote the pyramidal shape during the EDP etch. This nitride is stripped away after etching. A layer of PSG (C) is deposited and reflowed

to achieve planarity. Layer D in the figure above is doped poly, which circumscribes the emitter to form the gate. Next, another layer of PSG (E) is deposited, filling the structure with glass. Another poly layer (F) is deposited, forming the anode. The glass is then etched away, leaving a 2-3μm air gap between emitter and anode. This process does not provide vacuum encapsulation, so all device testing must be done in an evacuated chamber. The base of the pyramid is approximately 4 μm x 4μm. The estimated emission radius is 100nm.

Experimental results of this design are not available, but calculated values indicate current drive of approximately 1μA/tip and a g_m of approximately 1μS at a 55V anode voltage. This performance is comparable to that of the lateral emission device described earlier in the paper, and would suffer similar bandwidth constraints, even in emitter array form. However, since this structure is vertical, the achievable packing density would be greater in this design.

From a fabrication point of view, the long etch times to remove the sacrificial PSG have caused the researchers problems. This has necessitated a re-design of other parts of the structure to tolerate the extended etching times. Additionally, the vertical structure implies a very rough substrate topology. Even with re-flowed PSG, maintaining sufficient planarity for subsequent metallization of actual integrated vacuum circuits could be problematic. This particular device did not provide in-situ vacuum encapsulation, but the subject of the vacuum sealing of microcavities is well documented in literature [10].

PROPOSED WORK TO ADVANCE TOPIC

This section explores the potential for scaling these devices and creating useful system-level implementations. Potential problems are identified, and research directions to mitigate these problems are proposed.

Thermionic Applications and Limits of Scaling

As described earlier in the paper, integrated thermionic vacuum devices can be relatively easy to fabricate and integrate with standard IC processes and passive components. A functional integrated circuit has been demonstrated, which bodes well for successful implementation of other simple circuits. Even the need to heat the cathode to 1000^{o}K could be made more efficient by locally heating a submicron cathode.

There is, however, one characteristic of thermionic devices that will ultimately limit their scaling. Thermionic emission inherently limits device current density to approximately 0.5A/cm^2, which is about 200X smaller than metal to semiconductor contacts [6]. This will severely limit the potential applications of integrated thermionic devices because, for a given application, the necessary thermionic device will be much larger than a solid-state or field emission device with similar drive capability. In addition to the resulting low packing density of these devices, the large device size causes the transconductance to input capacitance ratio to be low, severely limiting the bandwidth of integrated thermionic devices.

Thus, integrated thermionic devices will most likely not be useful for high-performance applications. However, integrated thermionic devices are interesting vehicles for demonstrating proof-of-concept integrated vacuum circuits since they are easy to fabricate and integrate with passive components.

Field Emission Applications and Limits of Scaling

Although integrated vacuum field emission devices have not yet achieved the manufacturability or performance necessary for practical use, they hold a lot of promise for the future of integrated vacuum electronics. Due to the nature of their electron emission, field emission devices can achieve current densities commensurate with solid-state devices. A recent integrated field emission array exhibited a current density of 11.5A/cm^2, much higher than the theoretical maximum of a thermionic device [11]. The packing density of field emission devices is high, allowing the potential for large arrays and high levels of integration for practical applications.

As previously mentioned, there are formidable fabrication obstacles that must be surmounted before high levels of integration and performance are achieved. Vertical tips offer the highest packing density, and 3μm tip spacing is readily achievable. That dimension is ultimately scalable, but topography management with vertical structures will be important to make useful interconnect feasible for fully integrated systems.

Proposed Work

Up to now, most integrated vacuum electronics work has been device work. The research is still in the stage of publishing I-V curves, not transient signals, power consumption figures, or system-level performance. Now that integrated, micro-scale field emission and thermionic emission have been proven, more work needs to proceed on increasing the functionality of the devices before they can fulfill the requirements set out at the beginning of this paper. This section proposes research work that could potentially enable this technology to succeed in the aforementioned applications.

i.) Vertically Stacked Structures

There are a few characteristics of vacuum electronics that could potentially be exploited for a huge system-level benefit. One is that there is very little high-temperature fabrication involved in forming these devices. Also, the channel of the active device is a vacuum, not a precisely doped, pure, single crystalline substrate like solid-state devices. These observations open the door to new opportunities.

For example, it is possible to stack these structures vertically to dramatically increase the packing density. Because a single-crystalline substrate is not needed, deposited polycrystalline layers can be used for subsequent layers of active devices. Also, since the integrated thermal budget for each layer of devices would be small, and because there is no need for ultra-shallow junctions, there is no penalty for adding additional layers. See the following figure for a possible stacked vacuum device.

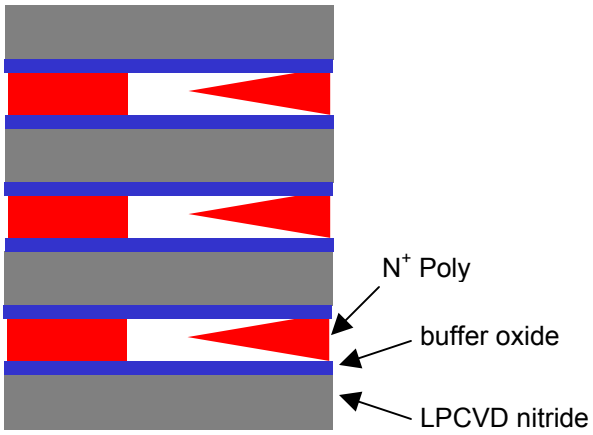

Figure 9. Possible Stacked Lateral Emitter Structure (cross section)

This device could be fabricated using a process flow similar to the lateral triode mentioned previously in this paper [8]. The sharpening oxidation would be done after all layers have been deposited. The main issue would be planarization, and research needs to be done to create a more planar device to be used as a building block of a stacked array. Planarization becomes increasingly important for successful lithography as the feature size of vacuum devices is decreased into the submicron regime. Another issue is that the vacuum encapsulation of these devices becomes increasingly difficult as the topography becomes more complicated.

Thermionic devices could also benefit from vertical fabrication. It has been identified that thermionic devices suffer from a very small current density (A/cm^2), limiting their usefulness in most applications. However, if the structure was built vertically instead of laterally, more surface area could be constructed for a given chip area, increasing the feasibility of a thermionic device. This would, however, undermine the easy IC-like fabrication that makes integrated thermionic devices so appealing in the first place.

ii.) Bottom-Up Approach to Field Emitter Fabrication

Another research area that could dramatically improve device performance and fabrication feasibility is a bottom-up approach to the emitter tip fabrication. This paper has reviewed many different methods for creating a sharp emitter tip. Most of these rely on traditional optical lithography to define some (or all) of the tip. Fabrication tricks are then used to further sharpen the tip. This process has proven to be difficult from a fabrication standpoint, unreliable from a device standpoint, and unusable from a circuit standpoint. A bottom-up approach for designing these nanometer scale features could provide a more convenient and reliable way of defining sharp and predictable emitter tips. For example, the selective growth of carbon nanotubes (CNTs) has been shown to be an effective field emitter. Preliminary work has shown the growth of CNTs with a 20-30nm diameter with field emission achieved with an anode voltage of 20V [12]. These results show promise that a bottom-up approach may finally solve the problem of creating a reliable, sub-lithographic sharp emission tip.

iii.) Improved Device Physics Modeling

In order to achieve higher performance out of integrated vacuum devices, more extensive device physics modeling must be utilized. So far, much effort has gone into the fabrication issues of these integrated vacuum devices. However, as large-scale fabrication of these devices becomes more feasible, accurate modeling of device performance will become crucial for their design and use. For example, more accurate modeling of the integrated triode will allow optimal placement of the grid electrode, thus allowing a higher device transconductance. This increases the gain and bandwidth of the device, making the device more practical from a system-level standpoint.

CONCLUSIONS

The field of integrated vacuum microelectronics has reached a point of maturity where device research leads to circuit- and system-level research. Only at that point can proof-of-concept circuits be designed and tested.

There are two main categories of vacuum electronics: thermionic emission and field emission. Integrated thermionic devices, while inefficient due to the cathode heater, can be a good way to demonstrate the functionality of microelectronic vacuum circuits and perfect the necessary vacuum encapsulation. Field emission devices offer better promise of scalability and the potential for high performance, but fabrication and device issues must be resolved before reliable systems can be built upon these devices.

New research exploiting the low thermal budget and vacuum channel of these devices could lead to their success in meeting the demands for a temperature tolerant, radiation hard active device.

REFERENCES

[1] De Forest, L. Patent 879,532 (U.S.)

[2] JPL/NASA Website: http://nppp.jpl.nasa.gov/asic/Appendix.3.html

[3] Orvis, W.J.; McConaghy, C.F.; Ciarlo, D.R.; Yee, J.H.; Hee, E.W. "Modeling and fabricating micro-cavity integrated vacuum tubes." IEEE Transactions on Electron Devices, vol.36, Nov. 1989. pp.2651-8.

[4] NASA Website: http://www.grc.nasa.gov/WWW/SiC/aircraftbenefit.html

[5] Svetlana Website: http://www.svetlana.com/docs/tubeworks.html

[6] Brodie, I.; Schwoebel, P.R.; Falk, H. "Vacuum microelectronic devices (and prolog)." Proceedings of the IEEE, vol.82, July 1994. pp.1005-34.

[7] Grigorishin, I.L.; Mukhurov, N.I.; Kotova, I.F. "Promising direction in making thermoradiation-resistant thermionic vacuum integrated microcircuits." IVMC '95. Technical Digest, IEEE, 1995. pp.385-9.

[8] Cheol-Min Park; Moo-Sup Lim; Byung-Hyuk Min; Min-Koo Han; Yearn-Ik Choi. "A novel lateral field emitter triode with insitu vacuum encapsulation." International Electron Devices Meeting, Technical Digest, IEEE, 1996. pp.305-8.

[9] Driskill-Smith, A.A.G.; Hasko, D.G.; Ahmed, H. "The "nanotriode:" A nanoscale field-emission tube." Applied Physics Letters, vol.75, AIP, Nov. 1999. pp.2845-7.

[10] Bartek, M.; Foerster, J.A.; Wolffenbuttel, R.F. "Vacuum sealing of microcavities using metal evaporation". Sensors and Actuators A, vol.A61, June 1997. pp.364-8.

[11] Whaley, D.R.; Gannon, B.M.; Smith, C.R.; Armstrong, C.M.; Spindt, C.A. "Application of field emitter arrays to microwave power amplifiers." IEEE Transactions on Plasma Science, vol.28, IEEE, June 2000. pp.727-47.

[12] Seong-Deok Ahn; Yoon-Ho Song; Sung-Yool Choi; Jong-Bong Park; Jung-Inn Sohn; Seong-Hoon Lee; Jin Ho Lee; Kyung-Ik Cho. "Gated carbon nanotube emitters grown on silicon trench wells with a sidewall spacer for stable vacuum microwave devices." IVMC 2001. Proceedings of the 14th International Vacuum Microelectronics Conference, IEEE, 2001. pp.55-6.