1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

*Fast Access Time -- 350 ns max.

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**

The Intel®2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (order as a 2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 42 mW maximum power dissipation in standby.*

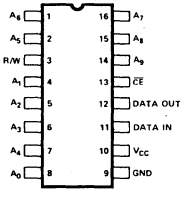
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

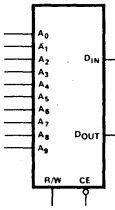
PIN CONFIGURATION

2102A



LOGIC SYMBOL

2102A



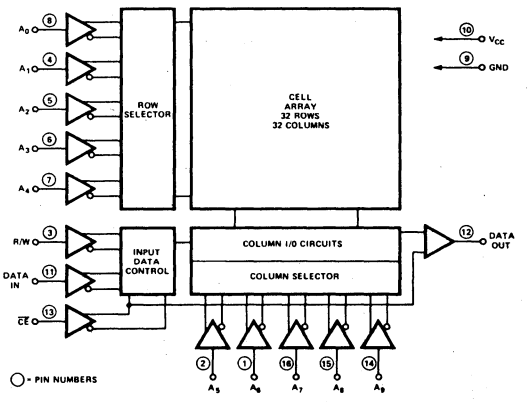
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

ORDERING INFORMATION

Maximum T_{ACC} & T_{CYC}	Standard Part No.	Standby-Mode Part No.
350ns	2102A	2102AL
250ns	2102A-2	2102AL-2
450ns	2102A-4	2102AL-4

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to + 70°C, V_{CC} = 5V ±5% unless otherwise specified.

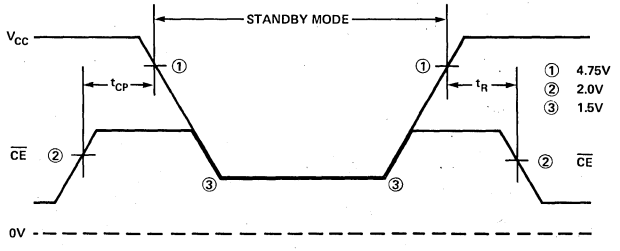
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}	Power Supply Current		30	60	mA	All Inputs = 5.25V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100μA

Standby Characteristics – See Ordering Information on Previous Page

T_A = 0°C to 70°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
V_{PD}	V_{CC} in Standby	1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			V	2.0V ≤ V_{PD} ≤ V_{CC} Max.
		V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
I_{PD1}	Standby Current Drain		15	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current Drain		20	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			ns	
t_R [3]	Standby Recovery Time	t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME).

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	350			ns
t_A	Access Time			350	ns
t_{CO}	Chip Enable to Output Time			180	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	350			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	250			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	250			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	250			ns

A.C. CONDITIONS OF TEST

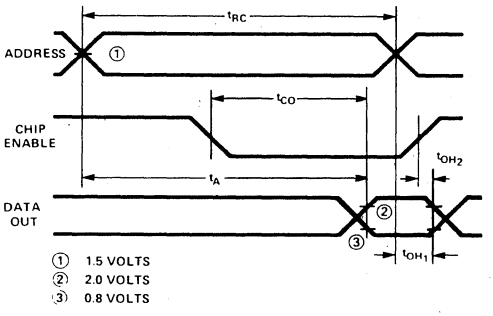
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

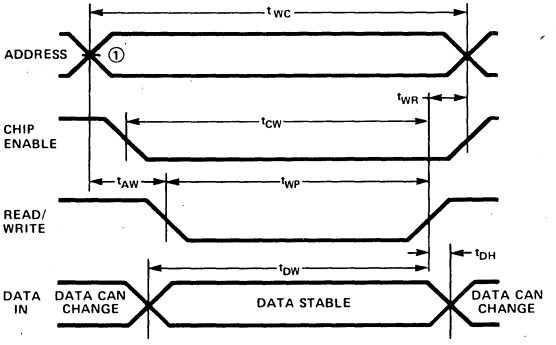
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



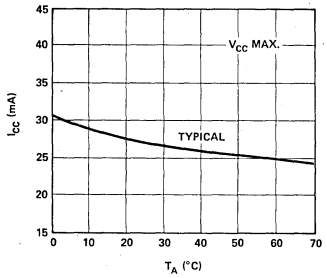
WRITE CYCLE



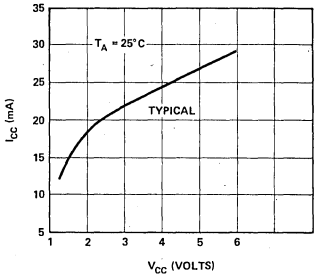
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

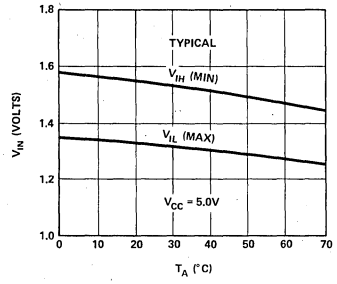
POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



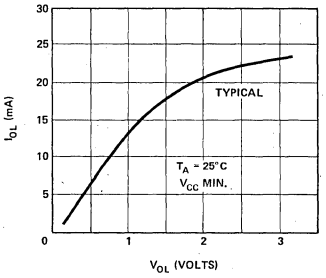
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



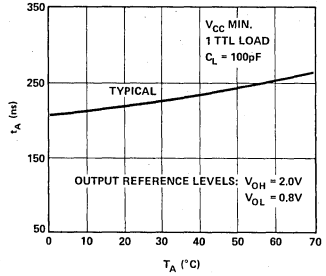
V_{IN} LIMITS VS. TEMPERATURE



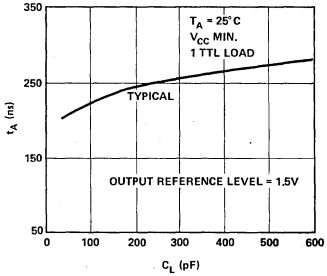
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



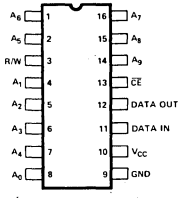
1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- ***Fast Access Time -- 250 ns max.**
- **Fast Cycle Time -- 250 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel®2102A-2 is a faster (250ns) version of the standard 2102A. It has all the same features, pin configuration, and D.C. operating characteristics as the standard 2102A. The absolute maximum ratings, pin configuration, and D.C. operating characteristics are repeated below for convenience, while the A.C. characteristics appear on the opposite side. *A low standby power version (order as a 2102AL-2) is also available. It has all the same operating characteristics of the 2102A-2 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)*

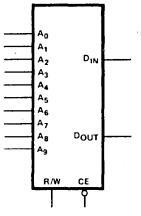
PIN CONFIGURATION

2102A-2



LOGIC SYMBOL

2102A-2



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}[2]	Power Supply Current		30	60	mA	All Inputs = 5.25V, Data Out Open, T_A = 25°C
I_{CC2}[2]	Power Supply Current			70	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. A low standby power version (order as a 2102AL-2) is also available. It has all the same operating characteristics of the 2102A-2 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	250			ns
t_A	Access Time			250	ns
t_{CO}	Chip Enable to Output Time			130	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	250			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	180			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	180			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	180			ns

A. C. CONDITIONS OF TEST

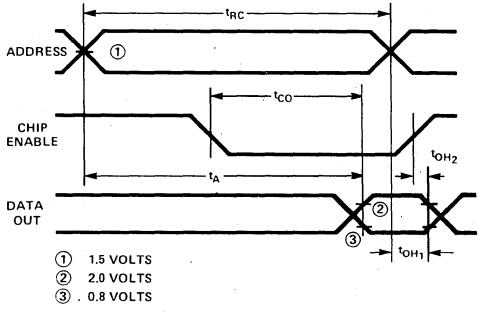
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

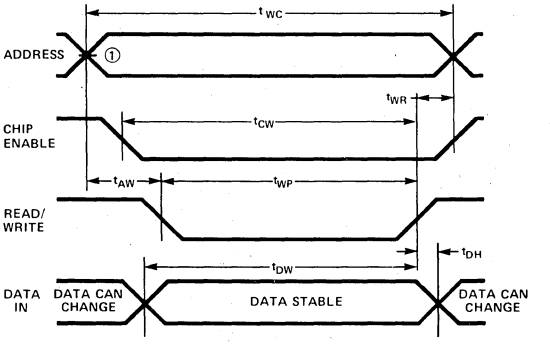
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

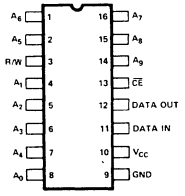
1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- **Fast Access Time -- 450 ns max.**
- **Fast Cycle Time -- 450 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel®2102A-4 is a 450ns version of the standard 2102A. It has all the same features, pin configuration, and D.C. operating characteristics as the standard 2102A. The absolute maximum ratings, pin configuration, and D.C. operating characteristics are repeated below for convenience, while the A.C. characteristics appear on the opposite side. *A low standby power version (order as a 2102AL-4) is also available. It has all the same operating characteristics of the 2101A-4 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)*

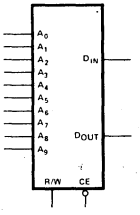
PIN CONFIGURATION

2102A-4



LOGIC SYMBOL

2102A-4



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}[2]	Power Supply Current		30	60	mA	All Inputs = 5.25V, Data Out Open, T_A = 25°C
I_{CC2}[2]	Power Supply Current			70	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. A low standby power version (order as a 2102AL-4) is also available. It has all the same operating characteristics of the 2101A-4 with the added feature of 42 mW maximum power dissipation in standby. (See 2102A data sheet for parametric definition.)

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

A. C. CONDITIONS OF TEST

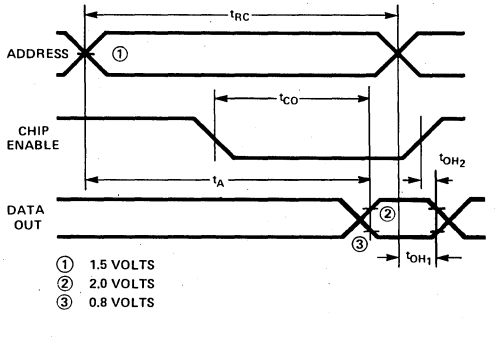
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

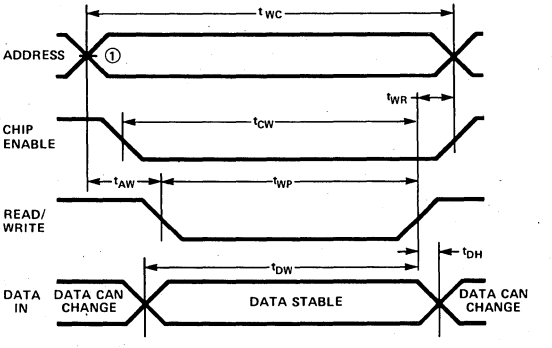
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

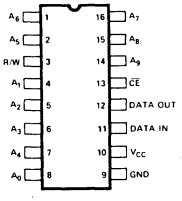
*Expanded Temperature Range--T_A = −55° C to +125° C

- ***Fast Access Time--450 ns max.**
- **Fast Cycle Time--450 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel® M2102A-4 is an expanded temperature range 1024 bit static N-channel MOS RAM. It is capable of operating over the full temperature range from −55°C to +125°C, and in addition the single 5 volt power supply can have a tolerance of ± 10%. The access time of the M2102A-4 is 450 nsec.

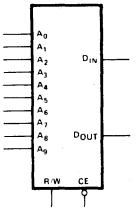
PIN CONFIGURATION

M2102A-4



LOGIC SYMBOL

M2102A-4



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . -55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output Leakage Current			10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.2 to V_{CC}
I_{LOL}	Output Leakage Current			-50	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	All Inputs = 5.5V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	All Inputs = 5.5V, Data Out Open, T_A = −55°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

A. C. CONDITIONS OF TEST

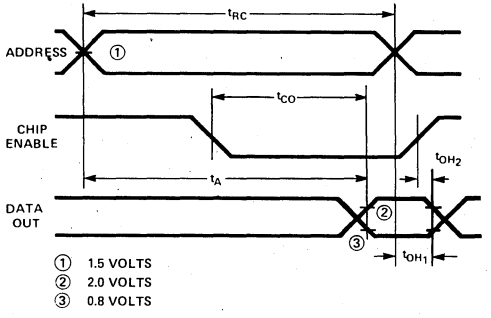
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1 MHz

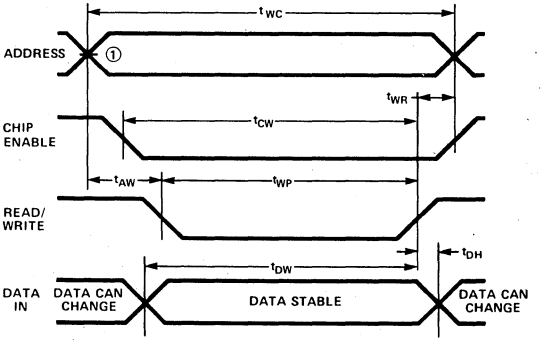
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

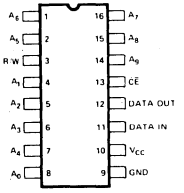
* Expanded Temperature Range: −55°C to +125°C

- **Fast Access Time--650 ns max.**
- **Fast Cycle Time--650 ns max.**
- **N-Channel Silicon Gate**
- **Maximum Times Apply over Temperature Range and Supply Voltage Variation**

The Intel®M2102A-6 is an expanded temperature range 1024 bit static N-channel MOS RAM. It is capable of operating over the full temperature range from −55°C to +125°C, and in addition the single 5 volt power supply can have a tolerance of ± 10%. The access time of the M2102A-6 is 650 nsec.

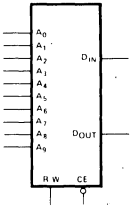
PIN CONFIGURATION

M2102A-6



LOGIC SYMBOL

M2102A-6



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	OUTPUT LEAKAGE CURRENT			−100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.5V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.5V DATA OUT OPEN T_A = −55°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.2		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 1.9mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	I_{OH} = −100μA

(1) Typical values are for T_A = 25°C and nominal supply voltage.

A. C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.[1]	MAX.	
READ CYCLE					
t_{RC}	READ CYCLE	650			ns
t_A	ACCESS TIME			650	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			400	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	650			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	200			ns
t_{WP}	WRITE PULSE WIDTH	400			ns
t_{WR}	WRITE RECOVERY TIME	50			ns
t_{DW}	DATA SETUP TIME	450			ns
t_{DH}	DATA HOLD TIME	100			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	550			ns

A.C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

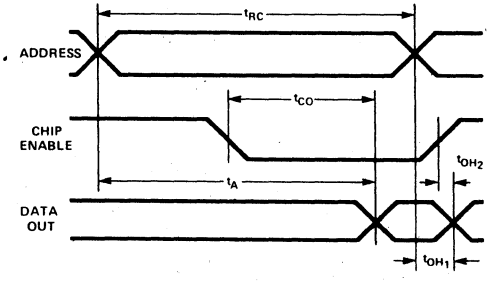
Output Load: 1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

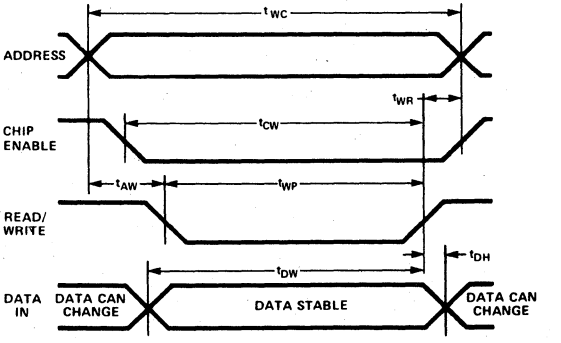
SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.