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MS-6555

Version 3.0

INTEL (R) 845GE/PE Chipset

Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale-G Chipset:

INTEL 845PE/GE + INTEL ICH4

On Board Chipset:

BIOS -- FWH

AC'97 Codec -- ALC201A

LPC Super I/O -- W83627HF

Clock Generation -- ICS950218AF

LAN -- RealTek 8100BL

ISA -- Winbond 83628 + 83629

Expansion Slots:

AGP2.0 SLOT * 1

PCI2.2 SLOT * 3

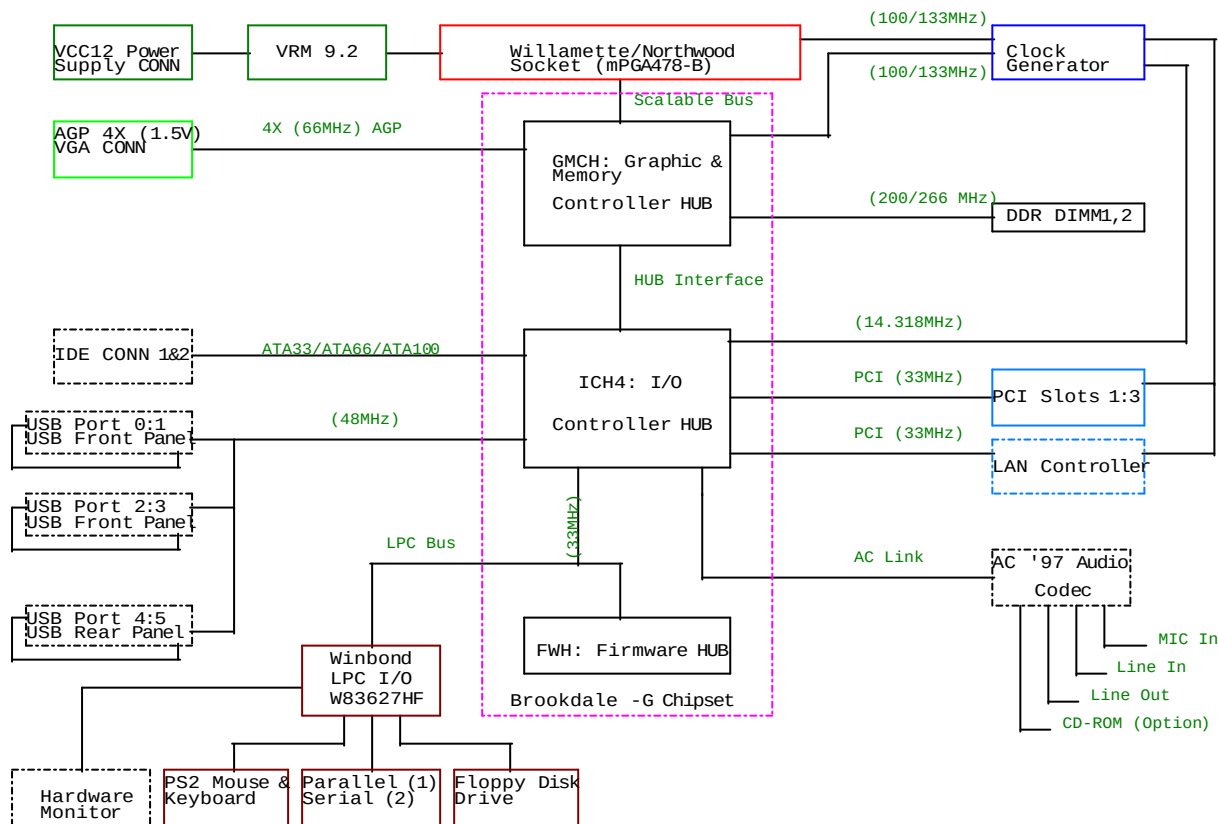
ISA SLOT * 1

Last Schematic Update Date:

Monday, August 19, 2002

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Title	COVER SHEET	Rev
Document Number	MS-6555	3.0
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Model option table

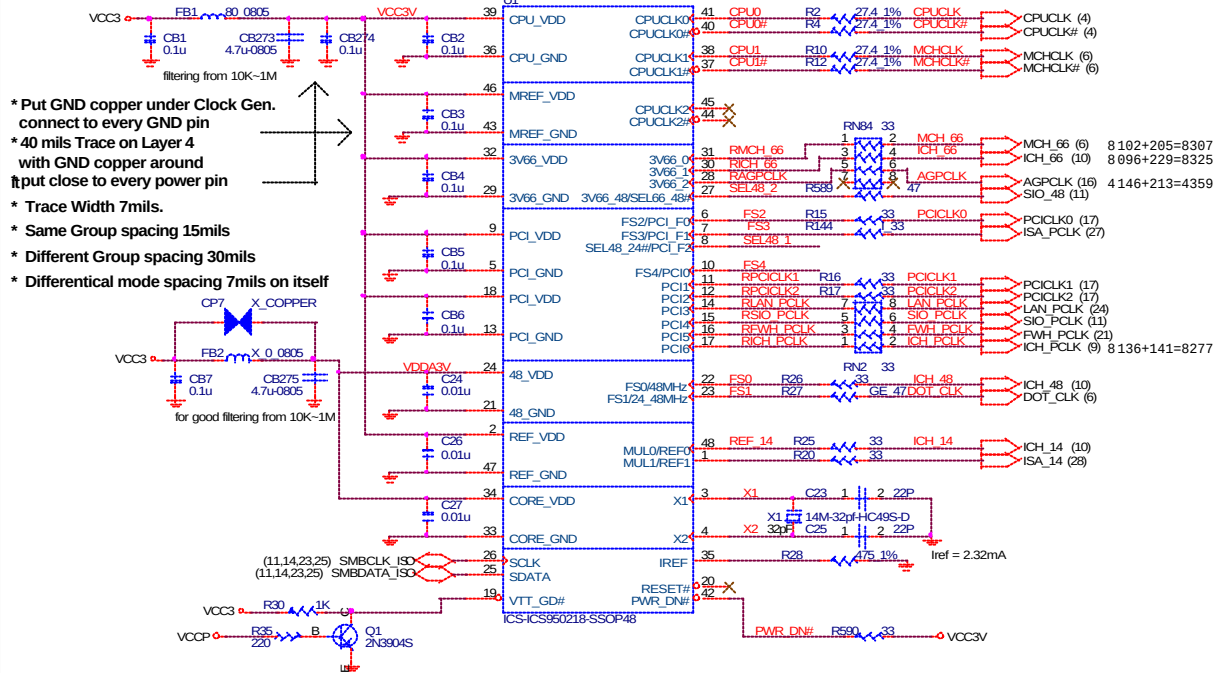
Model type	Function	BOM Config	ERP BOM No.
MS6555L2	For Legend (845PE)	Cfg6555L2-30-L	601-6555-04S

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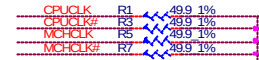
Title	BLOCK DIAGRAM	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, August 19, 2002	
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CLOCK GENERATOR BLOCK

*Trace < 0.5"



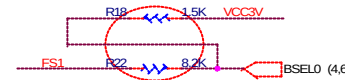
Shut Source Termination Resistors



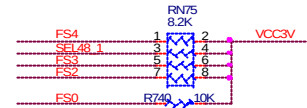
Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS

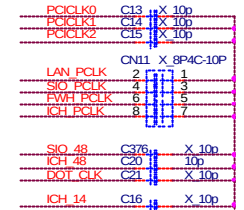


FS4	FS3	FS2	FS1	FS0	CPU (MHz)
1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz



MULTISEL0=0 -> 6X Iref
MULTISEL0=1 -> 7X Iref

Pull-Down Capacitors

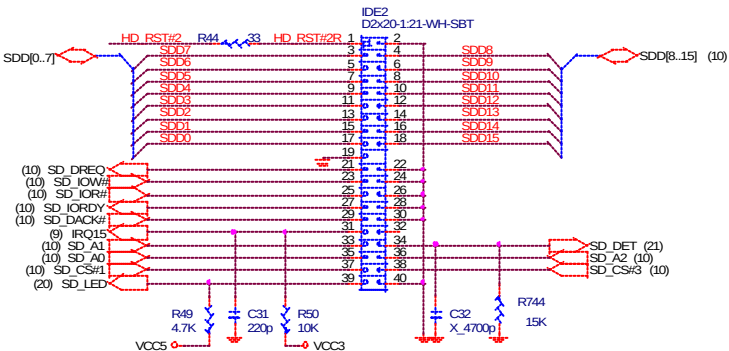
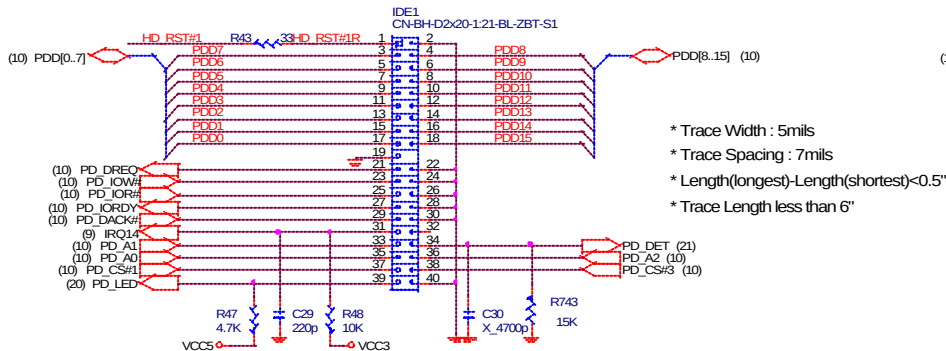


used only for EMI issue
Trace less 0.2"

PRIMARY IDE BLOCK

ATA100 IDE CONNECTORS

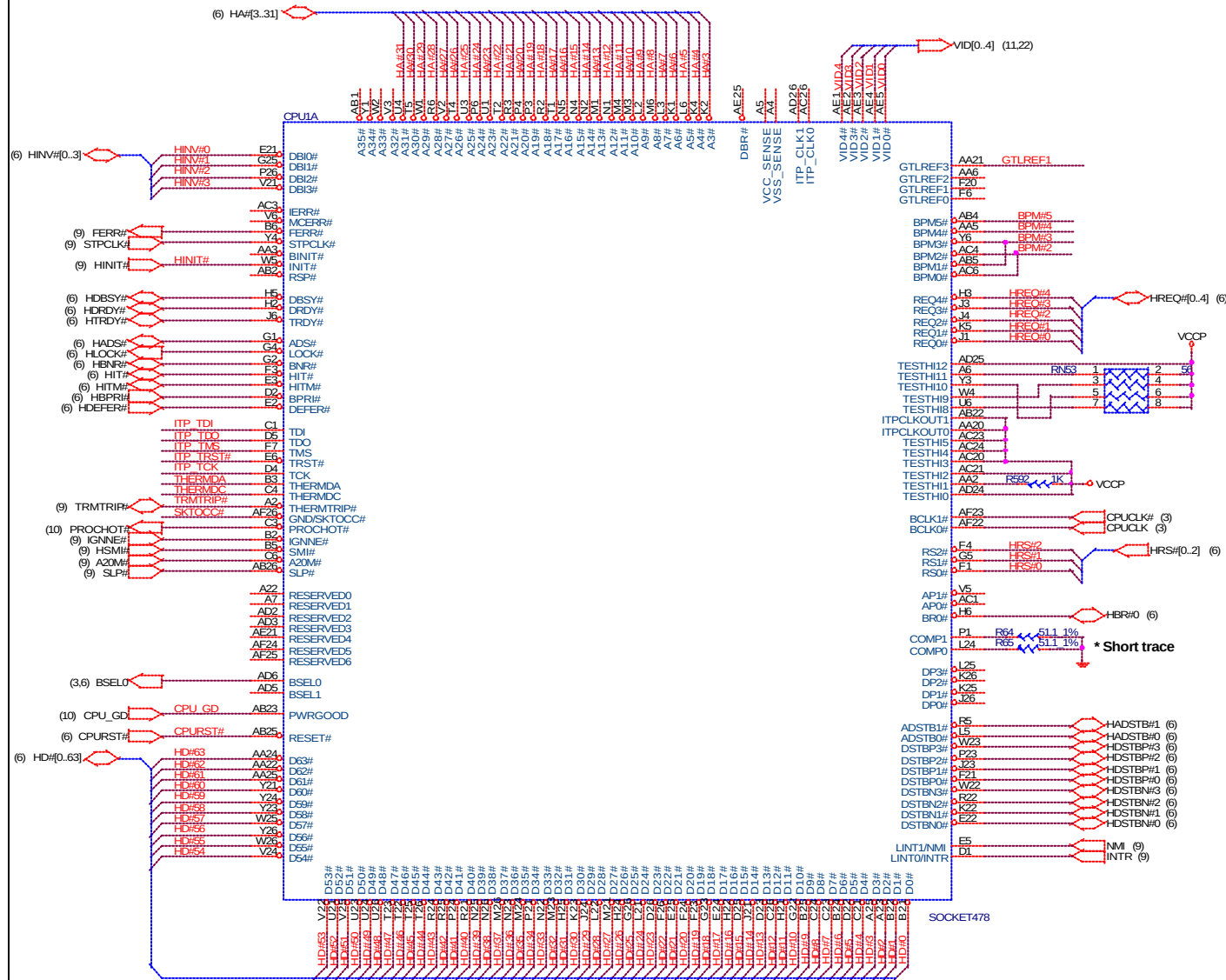
SECONDARY IDE BLOCK



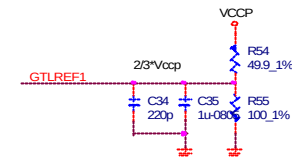
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Title	Clock & IDE Conn	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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CPU SIGNAL BLOCK

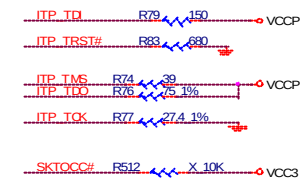


CPU GTL REFERENCE VOLTAGE BLOCK

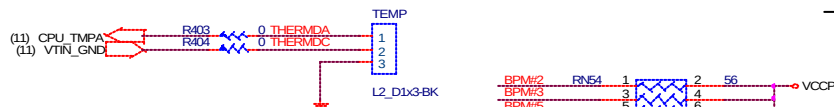


Every pin put one 220pF cap near it.
Trace Width 7mils, Space 10mils.
Keep the voltage divider within
1.5" of the GETREF pin.

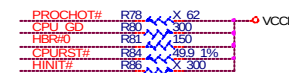
CPU ITP BLOCK



CPU STRAPPING RESISTORS



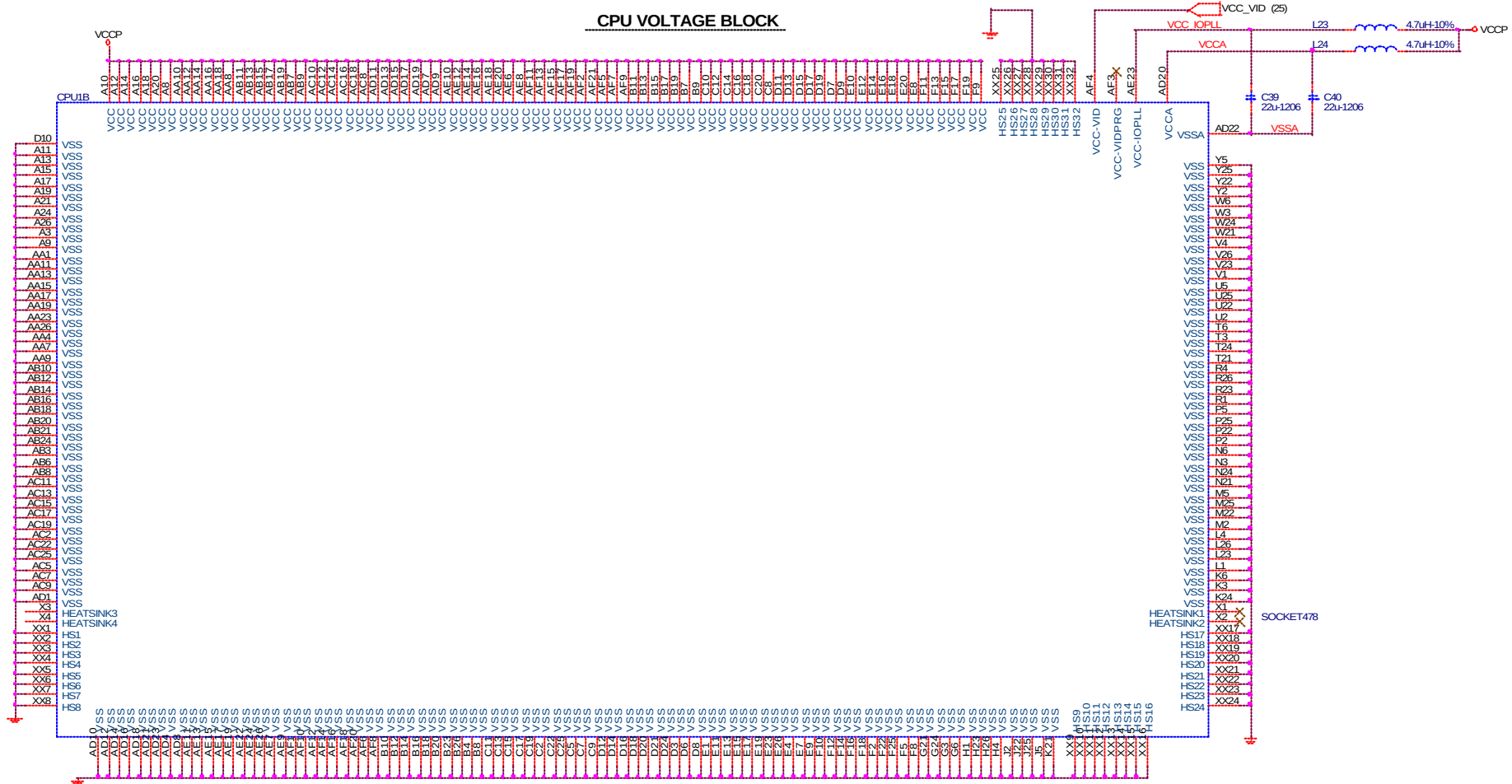
ALL COMPONENTS CLOSE TO CPU



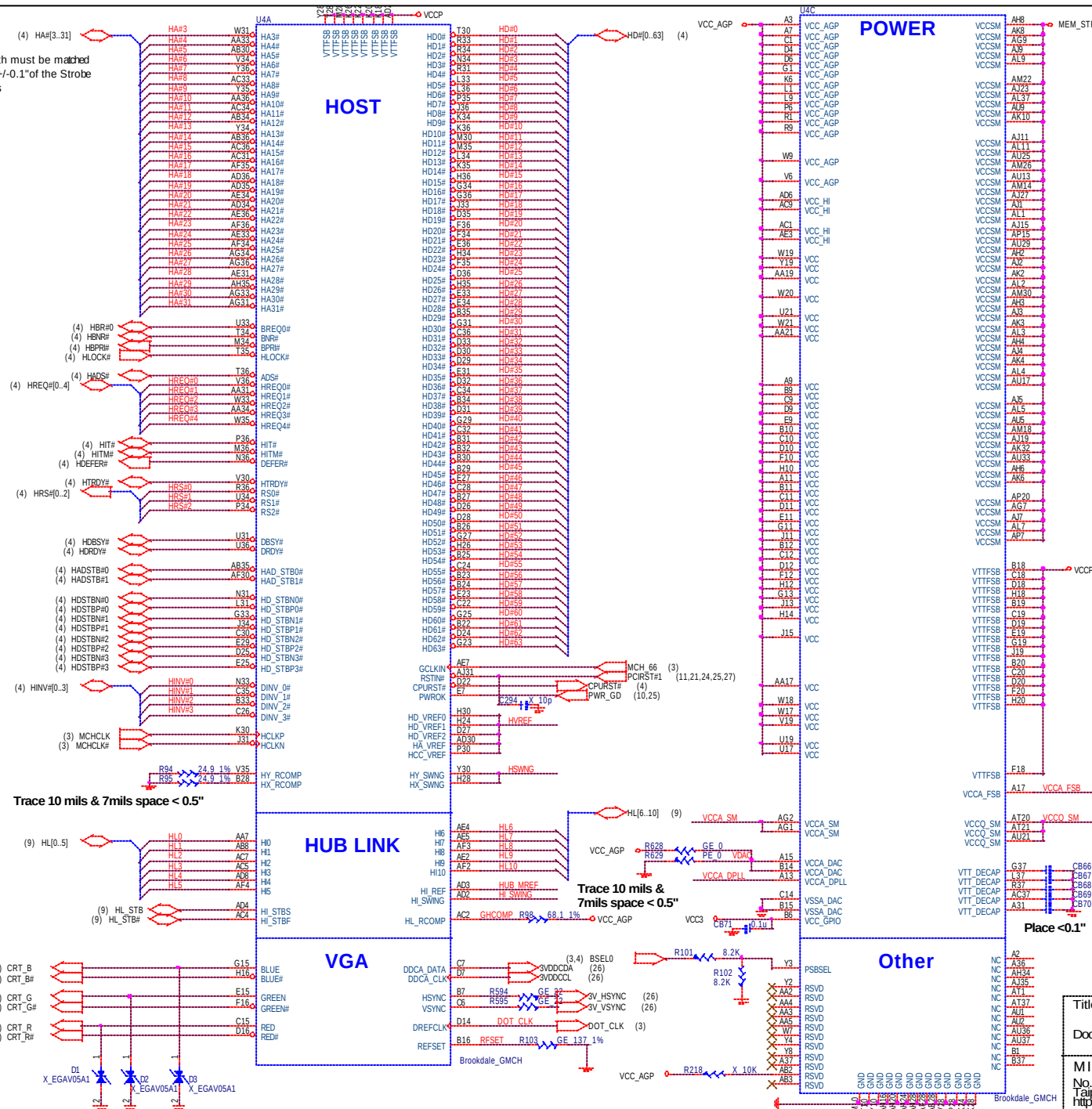
~~Micro Star Restricted Secret~~

Title		Rev	
mPGA478-B Intel CPU Socket Part 1			
Document Number	MS-6555	3.0	
MICRO-STAR INT'L CO., LTD.		Last Revision Date:	
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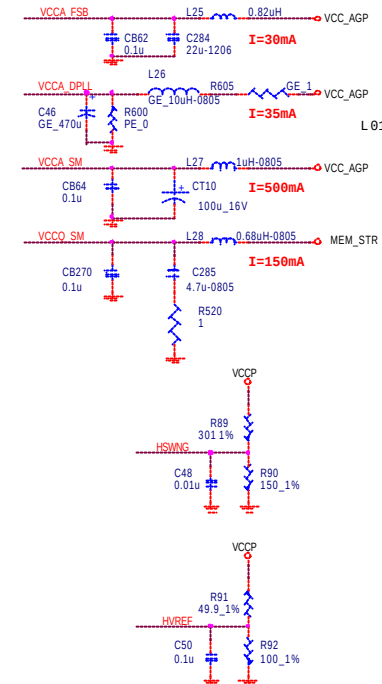
CPU VOLTAGE BLOCK



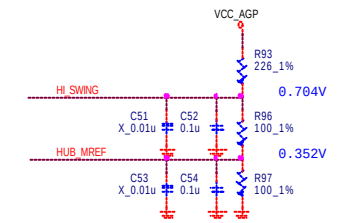
* Length must be matched within +/-0.1" of the Strobe Signals



GMCH REFERENCE BLOCK



Place Cap. as Close as possible to
GMCH , Trace width 12 mils & 10mils space
Keep the voltage divider within 3" of the
GMCH pin.

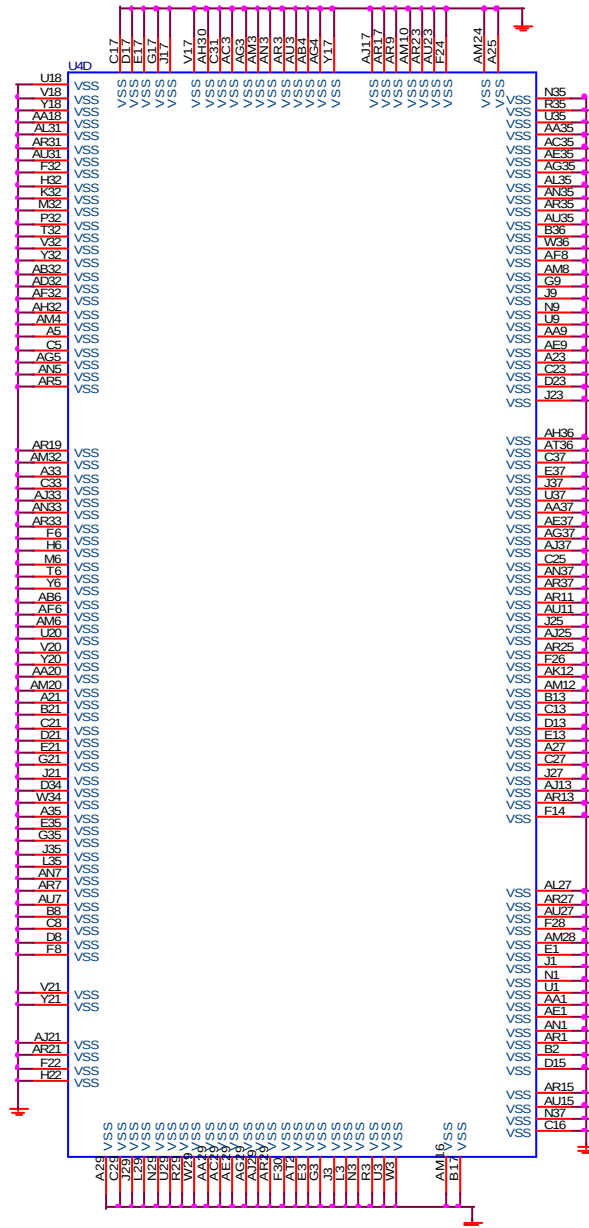


Place 0.01uF Cap. as Close as possible to
GMCH< 0.25"

Trace width 12 mils & 10mils space

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Title		Brookdale-G GMCH Part 1 (Power,Host ,VGA&HUB)		Rev	
Document Number		MS-6555		3.0	
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GMCH DECOUPLING CAPACITOR



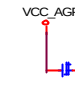
Pin A5
Pin E1
Pin J1
Pin N1
Pin U1

Place decoupling cap
close to GMCH AGP
Interface < 0.1"



Pin AA1
Pin AE1

Place decoupling cap
close to GMCH
Hub-Link Interface <
0.1"



Pin B14
Pin A15

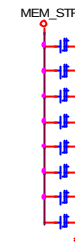
Place decoupling cap
close to GMCH DAC
Interface < 0.1"



Place decoupling cap
close to GMCH Core
Logic Interface <
0.1"

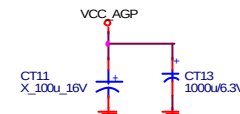


Place decoupling cap
close to GMCH CPU
Interface < 250mil
in the Vtt corridor

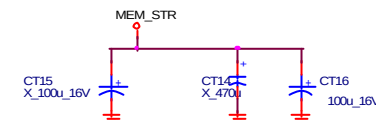
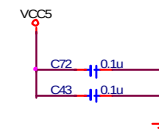
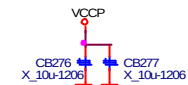


Pin AL37
Pin AU5
Pin AU9
Pin AU13
Pin AU17
Pin AU25
Pin AU29
Pin AU33

Place decoupling cap
close to GMCH Memory
Interface < 0.1", with
18 mil trace width



Place Bulk cap for Cpre Logic,
AGP & Hub Link Interface



Place Bulk cap between
GMCH & DIMM slot

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Title	Brookdale-G GMCH Part 3 (GND)		Rev
Document Number	MS-6555		3.0
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ICH4 SMI# SIGNAL

ICH4 STRAPPING RESISTORS

The diagram illustrates the strapping resistors for the ICH4. It shows three groups of pins connected to resistors, which are then connected to VCCP, VCC3, or ground.

- Group 1:** FERR# and TRMTRIP# are connected to R123 (62 ohms) and R124 (62 ohms), which are connected to VCCP.
- Group 2:** SERIRO, KB_RST#, ASIGATE#, and PREQWA are connected to R125 (8.2K), R126 (10K), R127 (10K), and R133 (10K), which are connected to VCC3.
- Group 3:** PREQWB, APIC_D0, APIC_D1, and APICLK are connected to R745 (10K), R128 (10K), and R129 (10K), which are connected to ground.

ICH4 REFERENCE VOLTAGE

The diagram shows a circuit for the ICH4 reference voltage. A vertical red line represents the VCC_AGP supply. Two resistors, R135 (226_1%) and R136 (100_1%), are connected in series between VCC_AGP and a central node. From this central node, two horizontal red lines branch out: HI_ISWING and HUB_IREF. Each horizontal line has a capacitor connected to ground (GND). The capacitor for HI_ISWING is labeled C80 (0.1u). The capacitor for HUB_IREF is labeled C82 (0.1u). The ground connections are marked with a red triangle and the label GND.

VCC_AGP

R135
226_1%

R136
100_1%

HI_ISWING

C80
0.1u

HUB_IREF

C82
0.1u

GND

GND

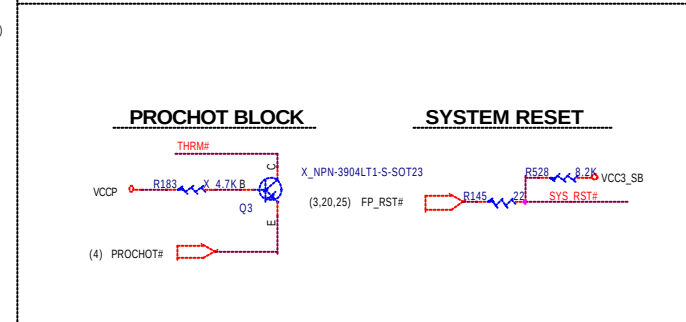
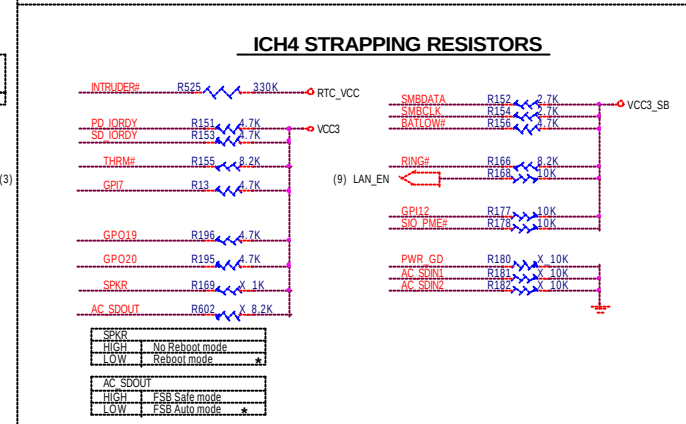
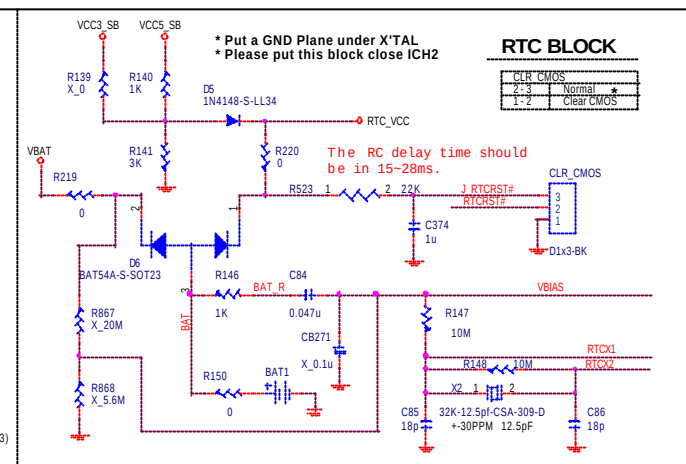
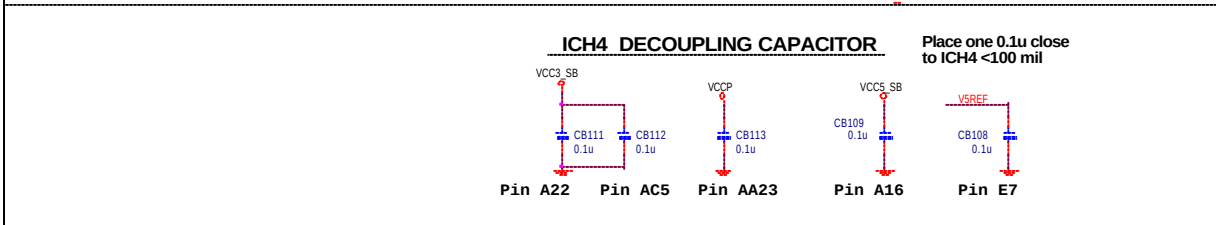
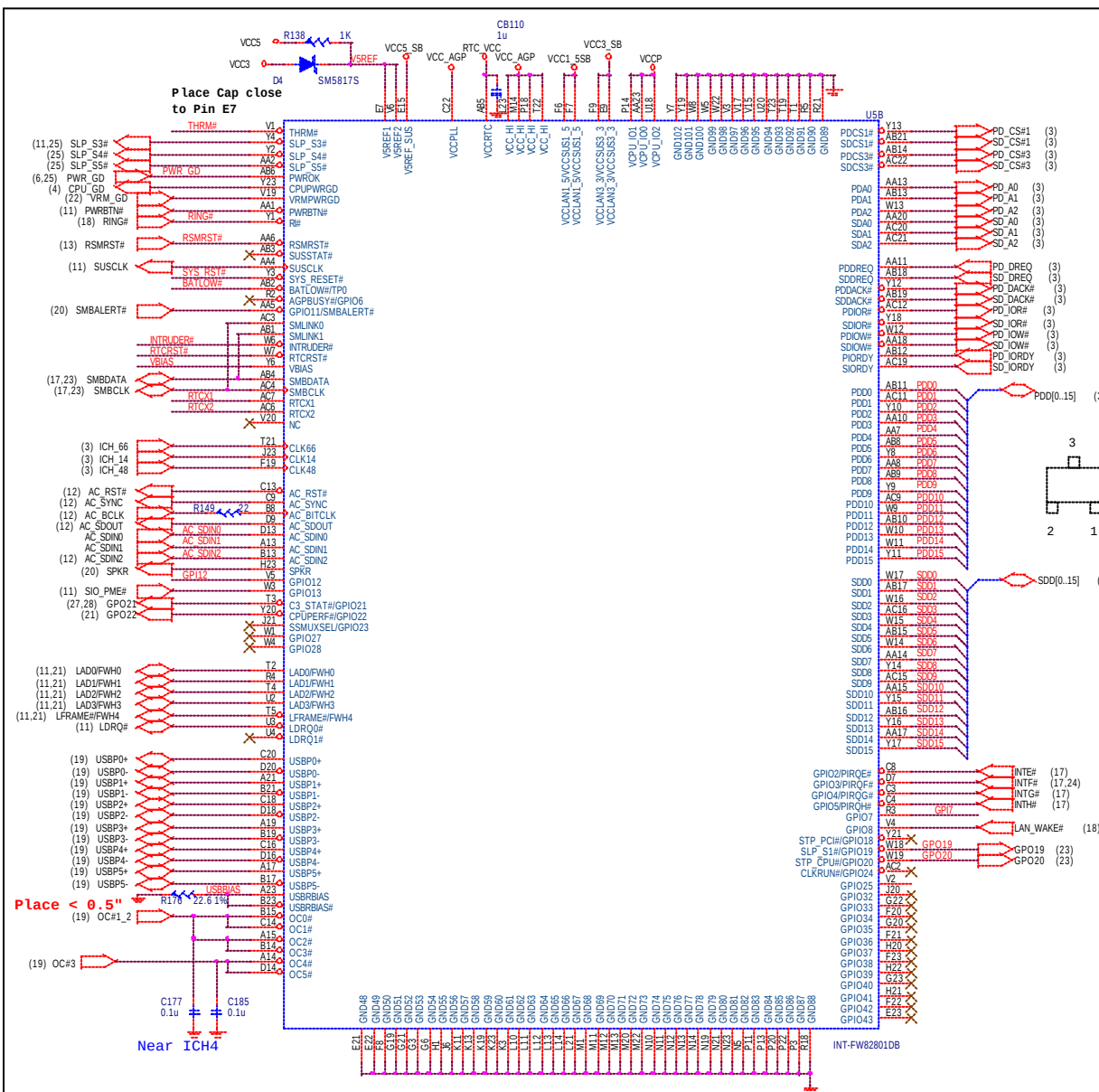
Place Cap. as Close as possible to ICH4 < 0.25"

Trace width use 12 mils and 10mils space

ICH4 DECOUPLING CAPACITORS Place one 0.1u close to ICH4 <100 mil

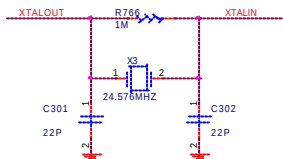
FOR Core Logic **FOR Hub Interface** **FOR PLL**

Title		Rev
ICH4 Part 1 (Power,HUB,PCI & CPU I/F)		
Document Number	3.0	
MS-6555		
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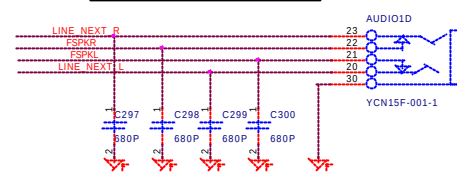


Title		Rev
ICH4 Part 2 (RTC,GPIO,LPC,USB,IDE)		3.0
Document Number		MS-6555
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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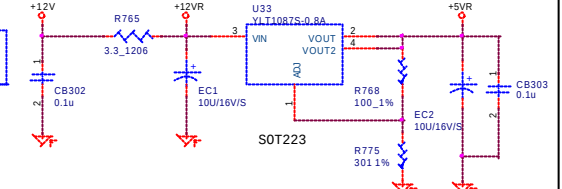
AUDIO CODE CRYSTAL CIRCUIT



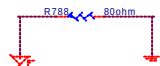
SPEAKER OUT JACK



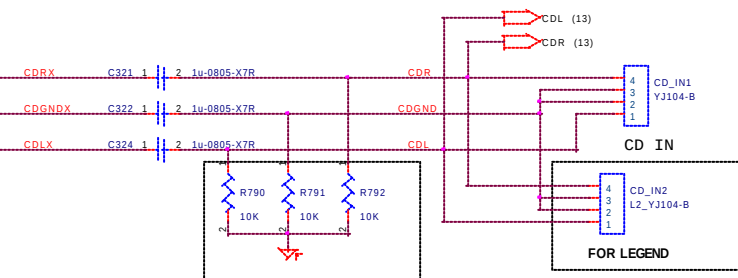
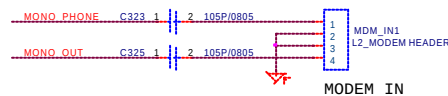
AUDIO CODEC REGULATORS



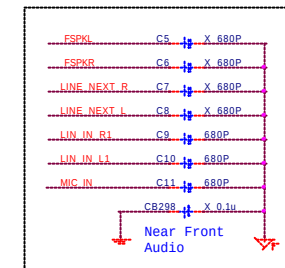
AD1881A AC97 CODEC



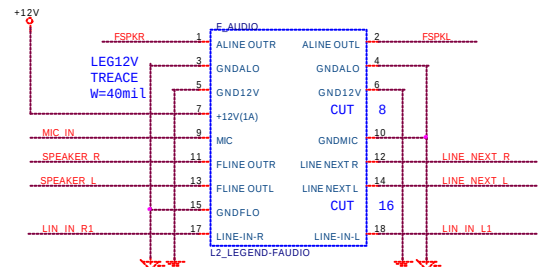
AUDIO CODE CD / AUX / MODEMINHEADERS



For EMI



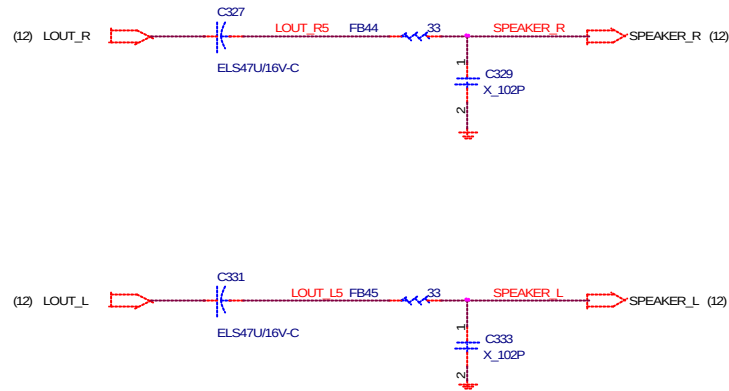
FOR LEGEND



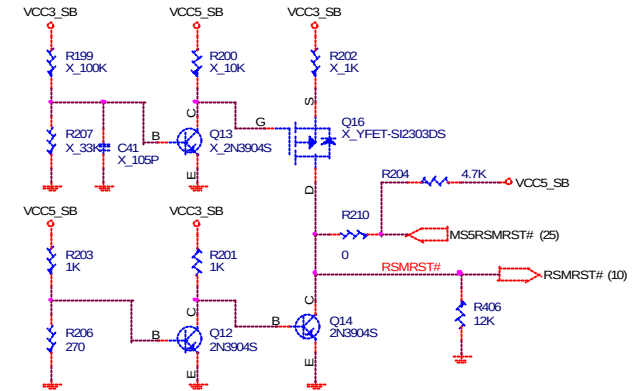
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Title	AC'97 CODEC	Rev
Document Number	MS-6555	3.0
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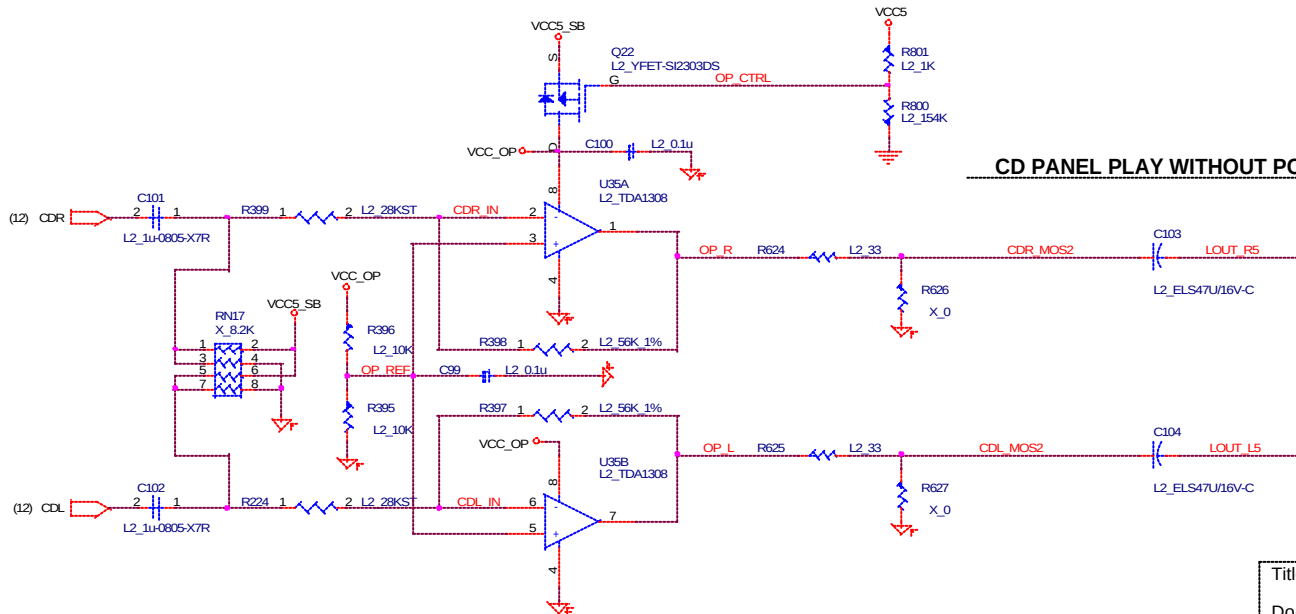
SPEAKER OUT CIRCUIT



Power-Well Isolation Control



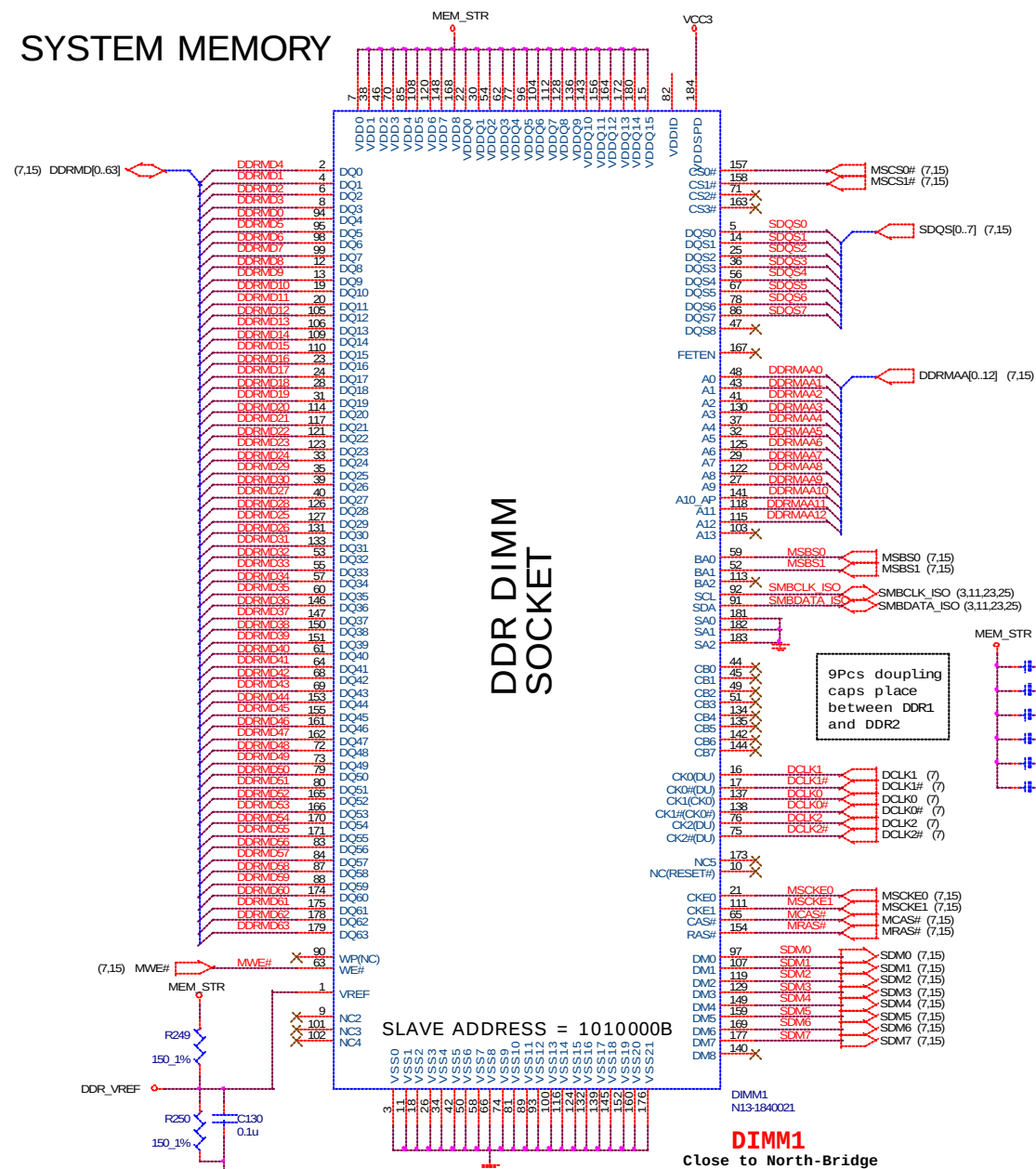
CD PANEL PLAY WITHOUT PC POWER ON



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Title	Audio Amplifier & CD Panel Play	Rev
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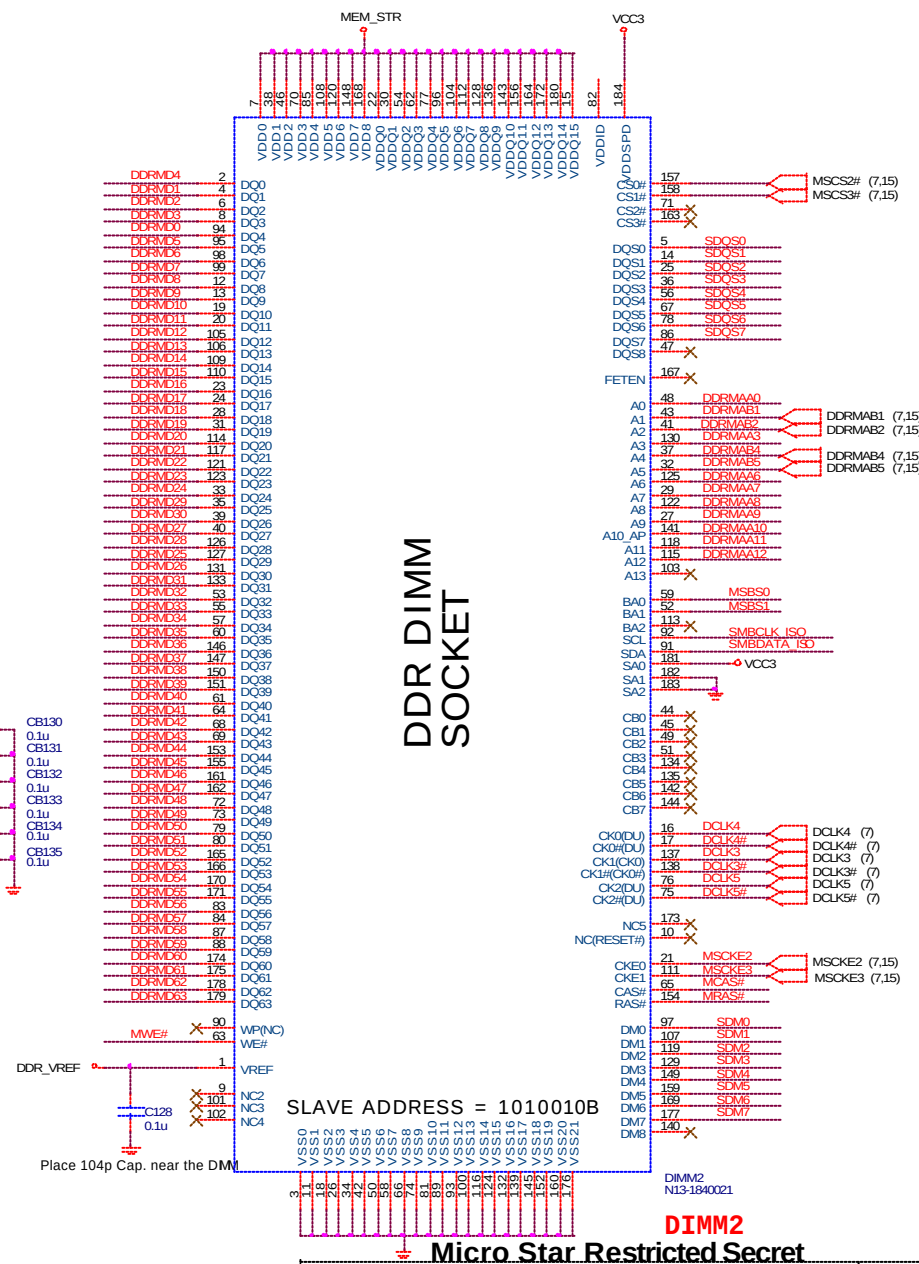
SYSTEM MEMORY



DDR DIMM SOCKET

DIMM1
Close to North-Bridge

Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
 Place 104p Cap. near the DMM



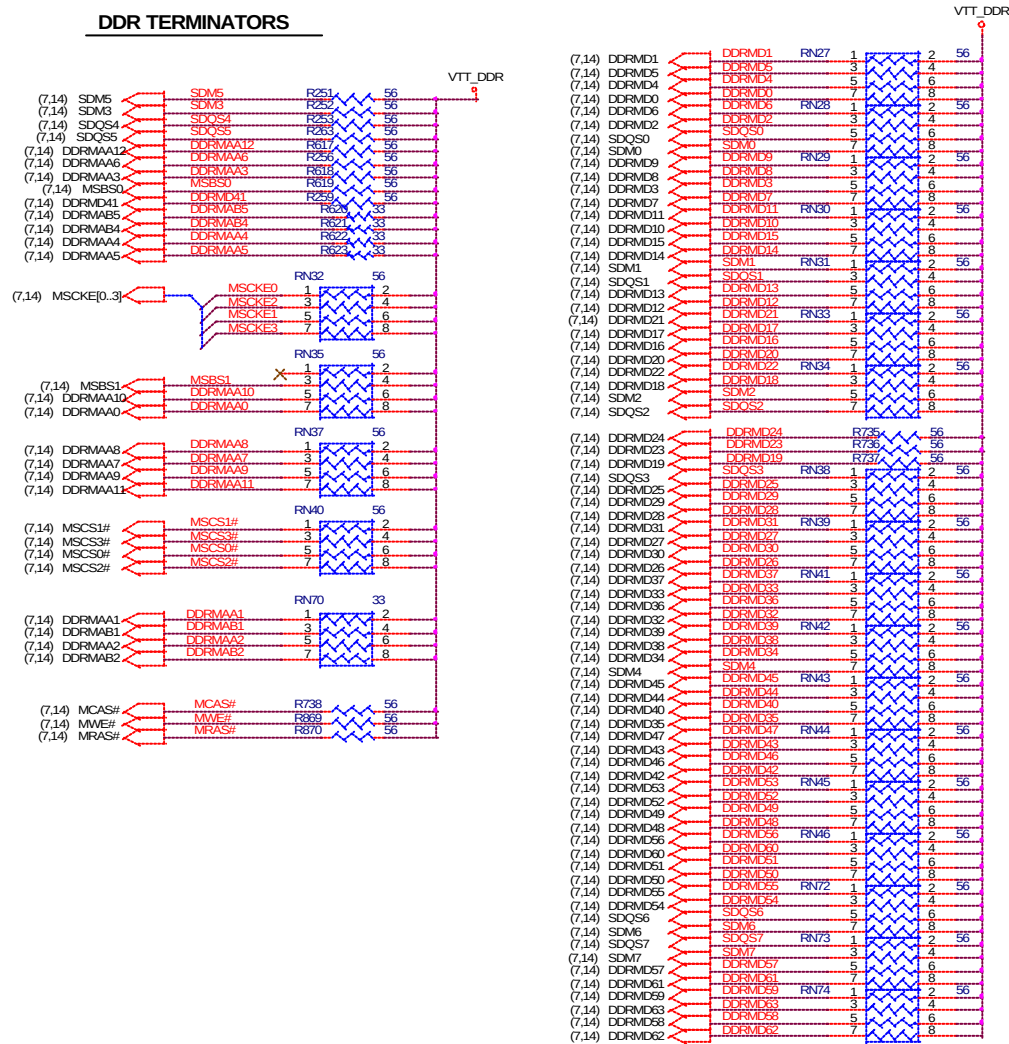
DDR DIMM SOCKET

DIMM2

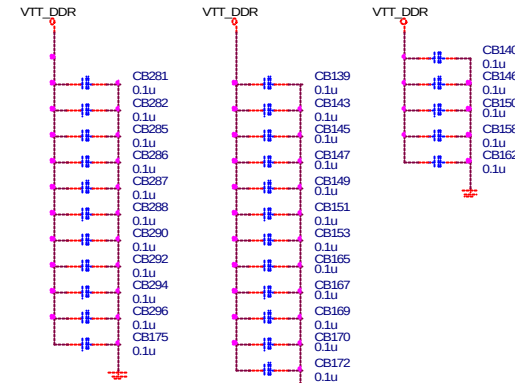
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Title		DDR DIMM 1 & 2	Rev
Document Number		MS-6555	3.0
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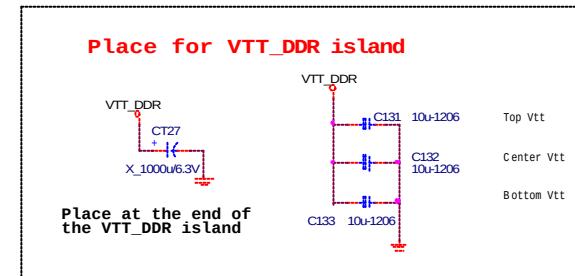
DDR TERMINATORS



DDR Decoupling Caps



Total 110 signal, need 55 pcs decoupling.



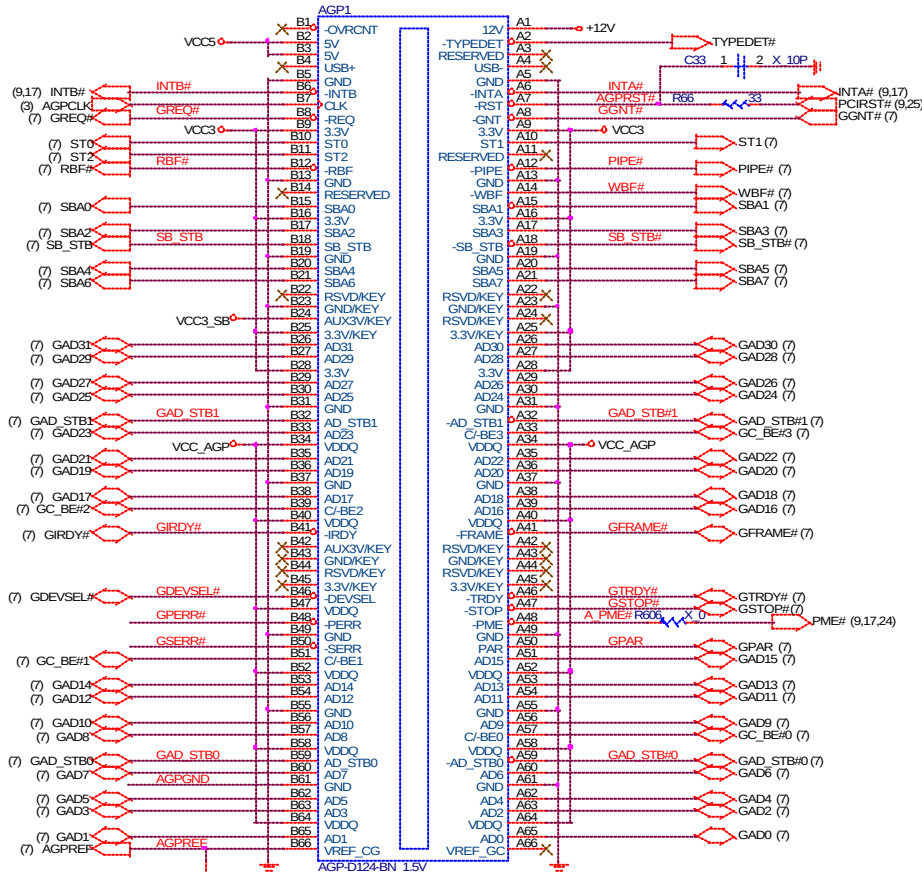
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Title		Rev
DDR Terminator Resistor		3.0
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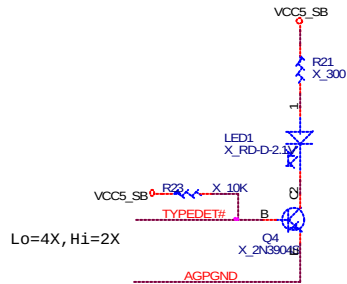
AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space

AGP Slot Imax
VCC_AGP 2.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A
VCC3_SB 0.375A

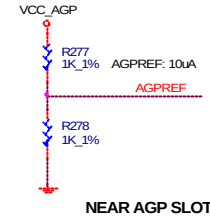


INTA# INTB#



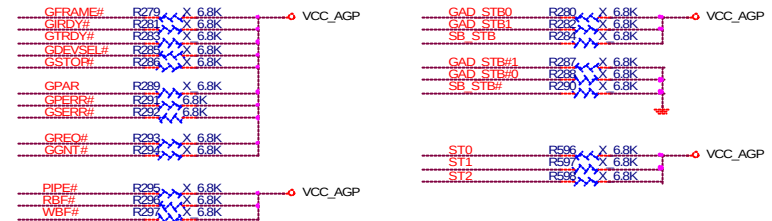
Lo=4X, Hi=2X

AGP SIGNAL REFERENCE CIRCUIT



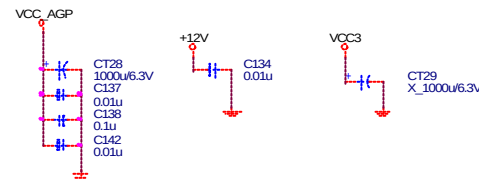
NEAR AGP SLOT

AGP TERMINATION RESISTORS



LESS 100MILS STUB TRACE LENGTH FOR 24X
LESS 500MIL FOR 1X MUST BE FOLLOWING
Place these resistors between AGP slot & GMCH

AGP SLOT DECOUPLING CAPACITORS



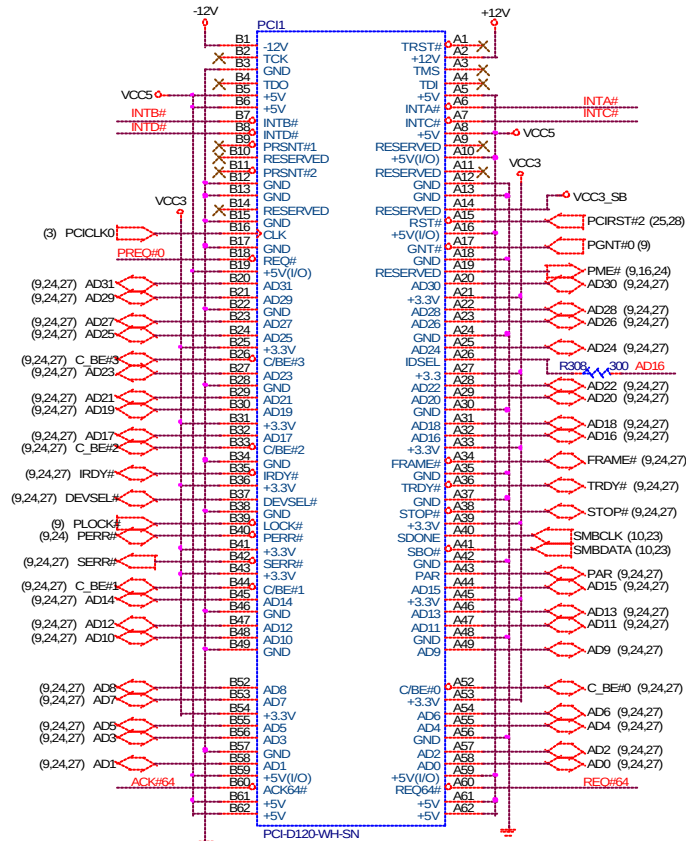
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Title	AGP 2.0	Rev
Document Number	MS-6555	3.0
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No. 69 Li-De St. Jung-He City, Taipei Hsien, Taiwan		Monday, August 19, 2002
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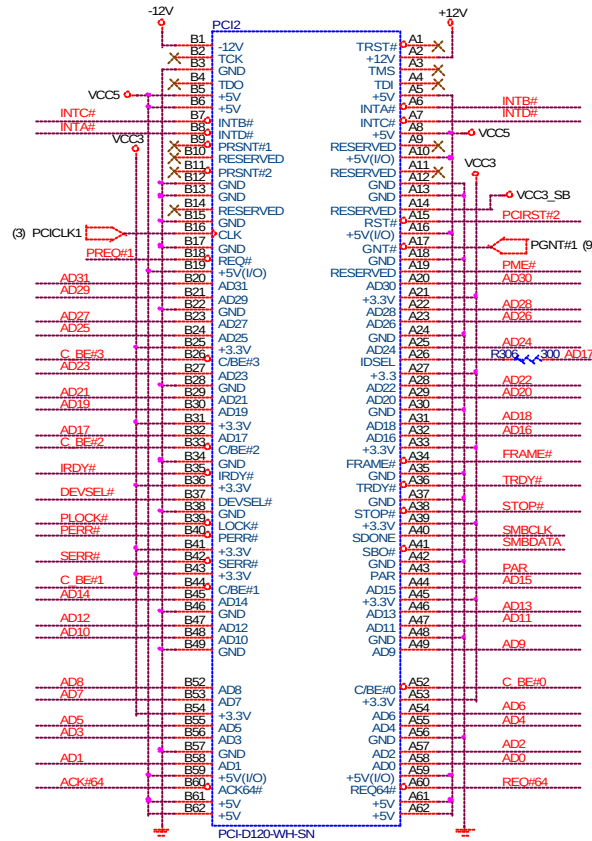
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

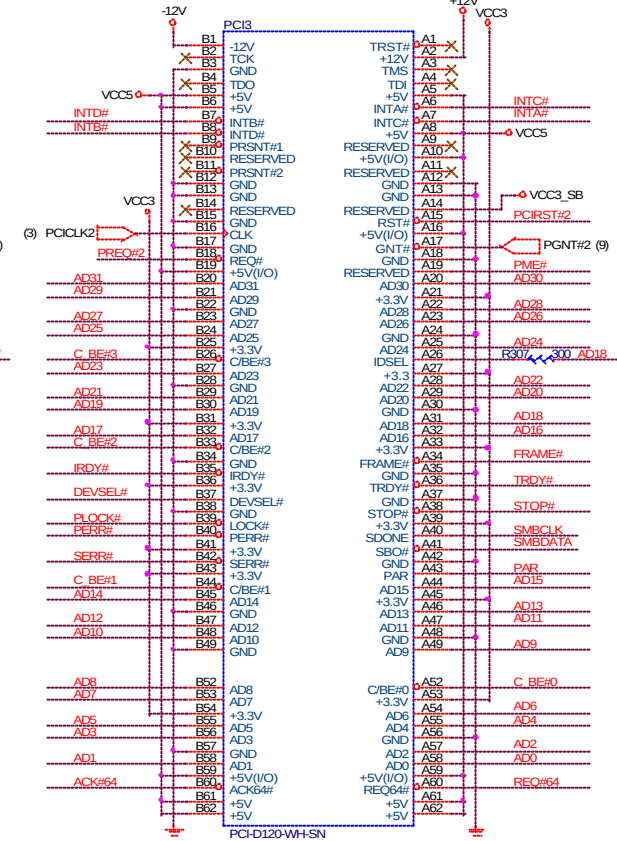
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ0
INTA#

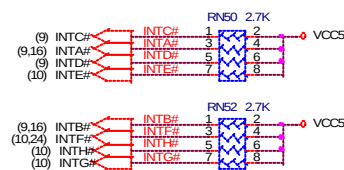
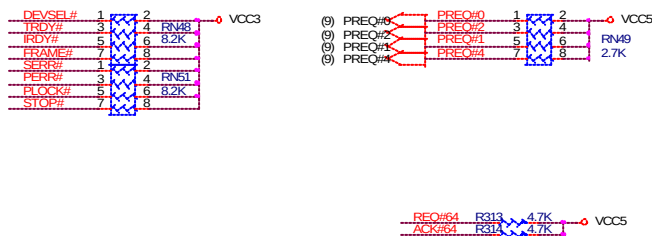


IDSEL = AD17
MASTER = PREQ1
INTB#

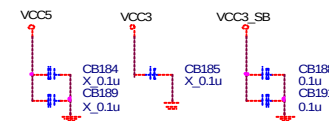


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

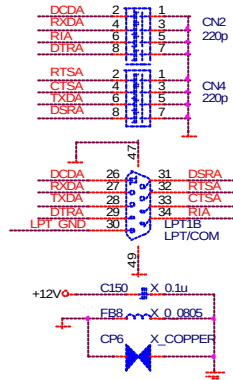


Micro Star Restricted Secret

Title	PCI SLOT 1 & 2 & 3	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
No. 69 Li-De St, Jung-He City, Taipei Hsien, Taiwan		Monday, August 19, 2002
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		17 of 31

SERIAL PORT 1

The schematic diagram illustrates the SERIAL PORT 1 circuit. It features a 75232L transceiver (U14) connected to two RS-485 bus nodes, CN2 and CN4. The transceiver is powered by VCC5 and GND, with decoupling capacitors C145 and C146. It has two differential signal pairs: DTRA/RTSA/TXDA and DTRS/RTSR/RXDA. Node CN2 (220pF) is connected to DTRA/RTSA/TXDA and DTRS/RTSR/RXDA. Node CN4 (220pF) is connected to DTRA/RTSA/TXDA and DTRS/RTSR/RXDA. The diagram also shows the connection of the transceiver to the RS-485 bus lines D9 and D10, which are terminated with 12V and 12V respectively.



SERIAL PORT 2

VCC5

U15

19 V+ 12VDC 0.1u

10 -12VDC 0.1u

75232-1

DCDB# (11)

RXDB# (11)

RIB# (11)

CTSB# (11)

DSRB# (11)

DTRB# (11)

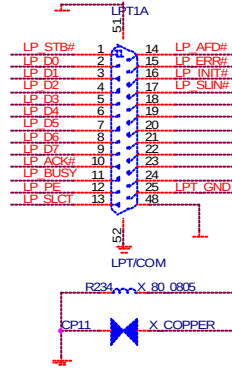
RTSB# (11)

SOUTB# (11)

COM2 HEADER

GE_D25-15-WH

LPTIC PE-LPT-D25-BK-BI

[illegible][illegible]

FLOPPY CONNECTOR

FDD01

Pin	Signal	Direction
1	DRVEND0	Output (11)
2	DRVEND1	Output (11)
3	INDEX#	Input (11)
4	MOT A#	Input (11)
5	DRV B#	Input (11)
6	DRV A#	Input (11)
7	MOT B#	Input (11)
8	DIR#	Input (11)
9	STEP#	Input (11)
10	WT DT#	Input (11)
11	WT EN#	Input (11)
12	TRACK#	Input (11)
13	FDD WP#	Input (11)
14	RDAT#	Input (11)
15	HEAD#	Input (11)
16	DSKCHG#	Input (11)
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		

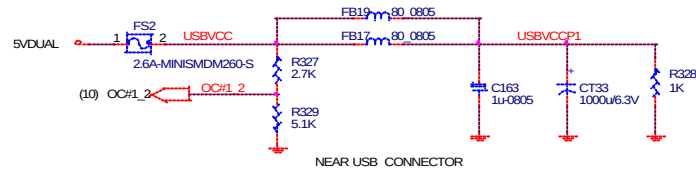
D2x17-3:20,29,31

Wake On Modem Header

The schematic diagram illustrates the Wake On Modem Header circuit. It features a WOMB (Wake On Modem Board) with pins 1, 2, and 3. Pin 1 is connected to L2_D1x3-BK. Pin 2 is connected to VCC5_SB. Pin 3 is connected to C306 (X_104P). The circuit includes a 1N4148-S-LL34 diode (D24, D25), a 10K resistor (R193, R194), a 10K resistor (R803, R804), a 2N3904S transistor (Q6), a 2N3906S transistor (Q64), and a 10K resistor (L2_330). The output is RING# (I/O).

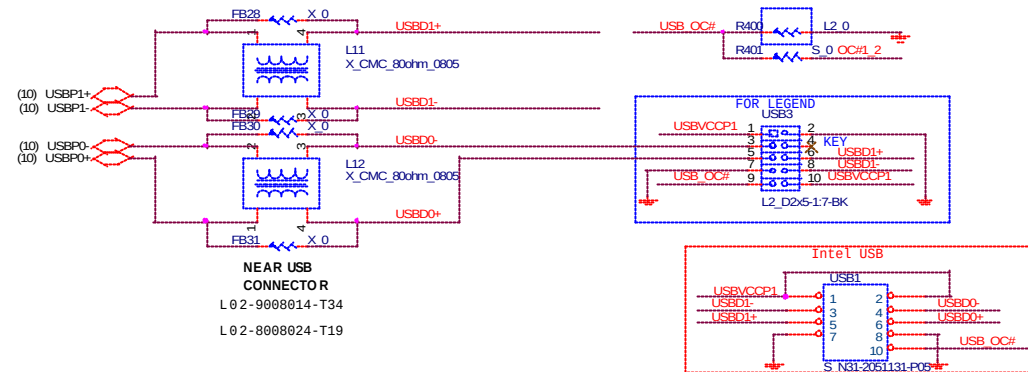
		Wake On LAN Header
Micro Star Restricted Secret		
Title KB,MS,SERIAL,PARALLEL & FLOPPY	Rev 3.0	
Document Number MS-6555		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, August 19, 2002	
Sheet 18 of 31		

POWER CIRCUIT FOR USB PORT 0,1



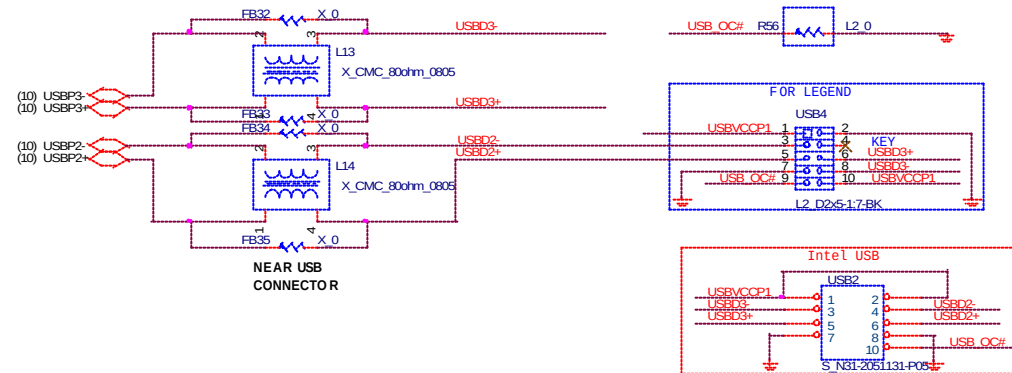
- * USB Trace width : 7.5 mils
- * USB Trace Spacing : Low speed 20 mils, High speed 50 mils
- * Differential USB Signlas Trace, Spacing : 7.5 mils
- * USB Power Trace must be 40mils width
- * Length(longest)-Length(shortest)<150mils
- * Maxium trace length <5"

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

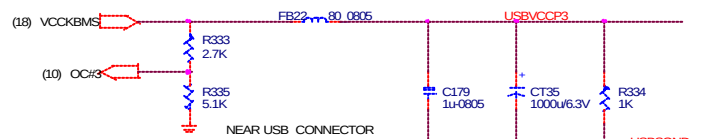


For MSI Bluetooth / Wireless Pin Header

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

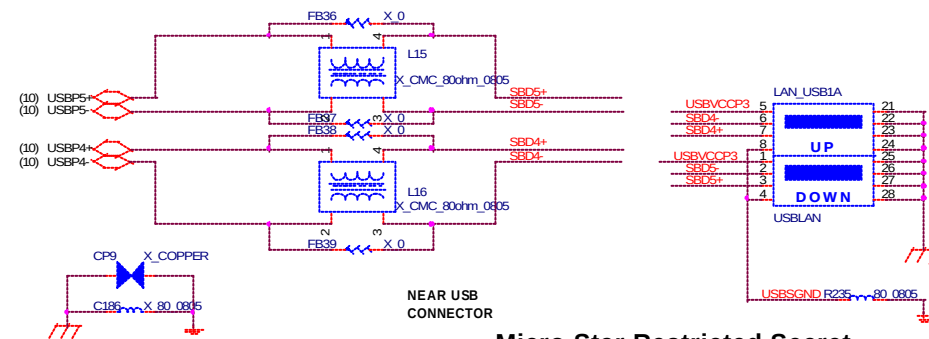


POWER CIRCUIT FOR USB PORT 4,5



- * USB Trace width : 7.5 mils
- * USB Trace Spacing : Low speed 20 mils, High speed 50 mils
- * Differential USB Signlas Trace, Spacing : 7.5 mils
- * USB Power Trace must be 40mils width
- * Length(longest)-Length(shortest)<150mils
- * Maxium trace length <16"

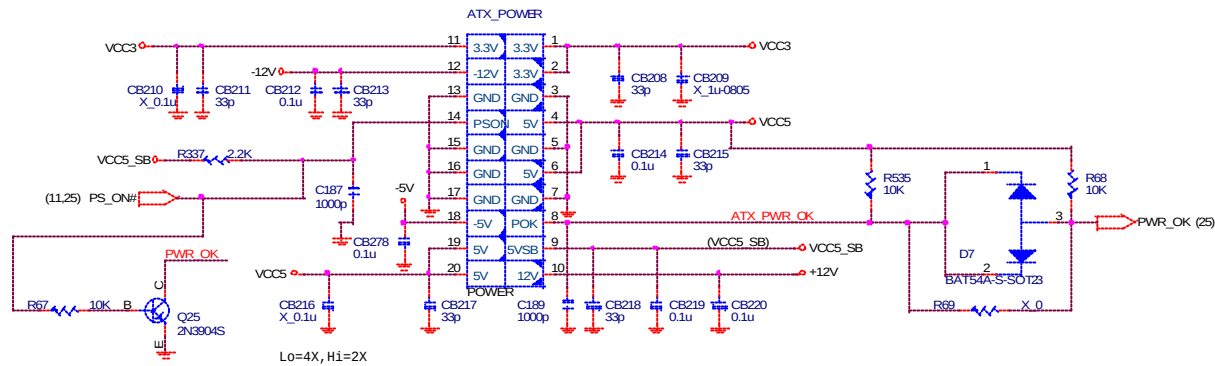
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



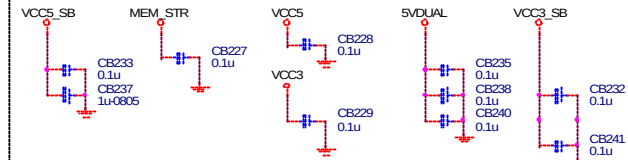
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Title	USB Connectors	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
No. 69 Li-De St, Jung-He City, Taipei Hsien, Taiwan		Monday, August 19, 2002
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ATX CONNECTOR

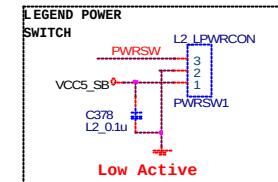
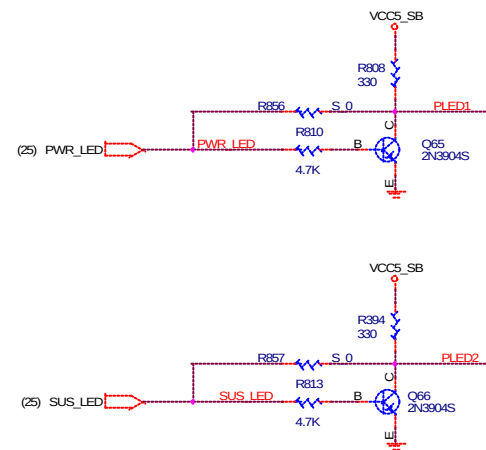
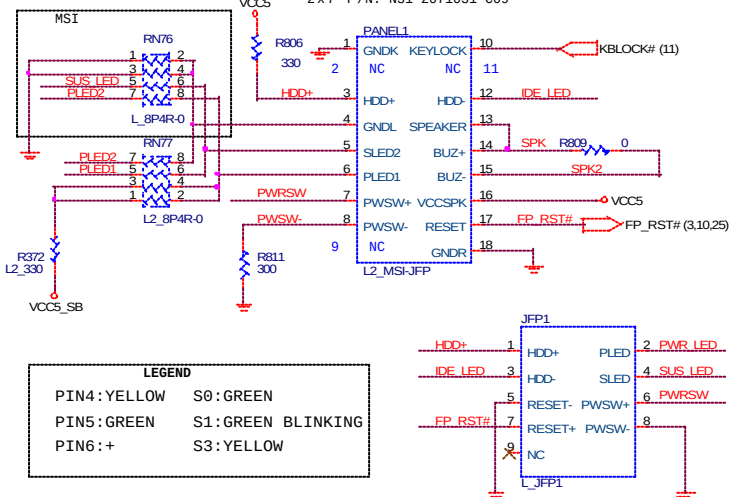


REGULATORS OUTPUT DECOUPLING CAPACITORS



MSI/Legend Front Panel

2x9 P/N: N31-2093011-C09
2x7 P/N: N31-2071031-C09

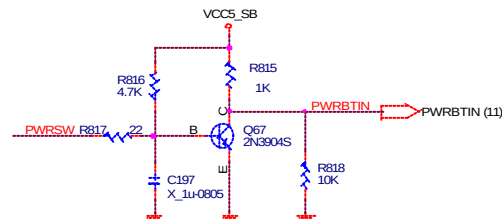


LEGEND DUAL

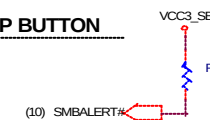
+ GREEN
- YELLOW

S0: STEADY GREEN
S1: GREEN BLINKING
S3: STEADY YELLOW
S4/S5: OFF

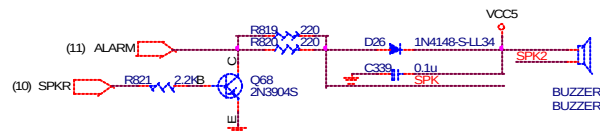
POWER BUTTON



SLEEP BUTTON



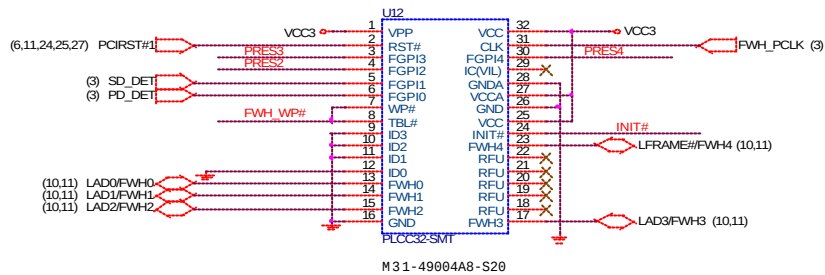
SPEAKER



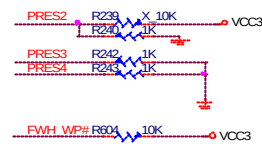
Micro Star Restricted Secret

Title	Front Panel, Power Conn. & Speaker	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
No. 69 Li-De St. Jung-He City, Taipei Hsien, Taiwan		Monday, August 19, 2002
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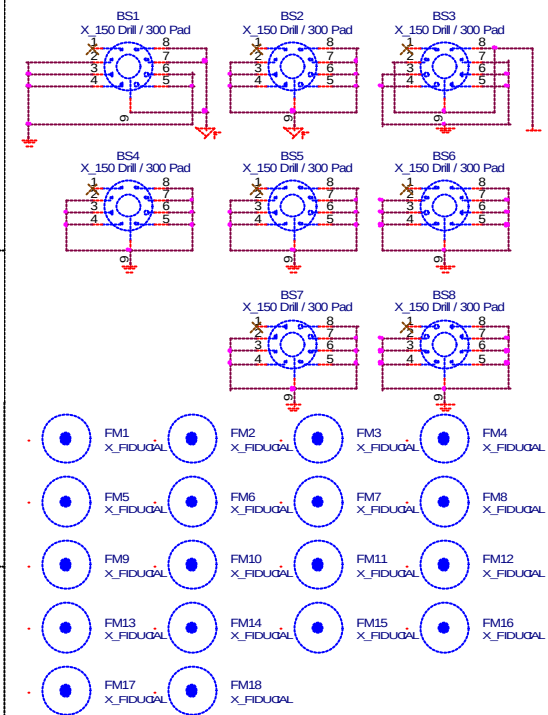
Firmware Hub (FWH)



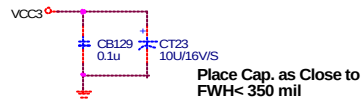
FWH RESISTORS



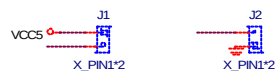
PCB OTHER COMPONENT



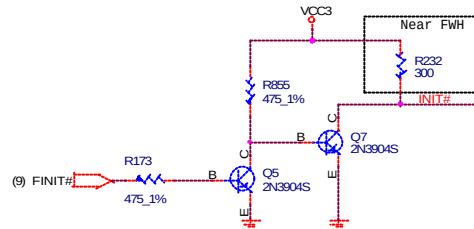
FWH DECOUPLING CAPACITORS



SIMULATION TRACE



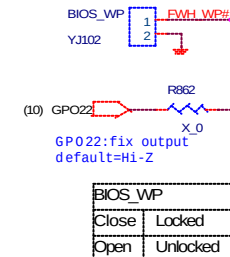
FWH INIT Signal Voltage Translation Block



CNR RISER

- * LAN Trace width : 5 mils
- * AC'97 Trace Spacing : 10 mils
- * Maximum trace length < 9.5"
- * Equal to or up to 500 mils shorter than the ELAN_CLK trace

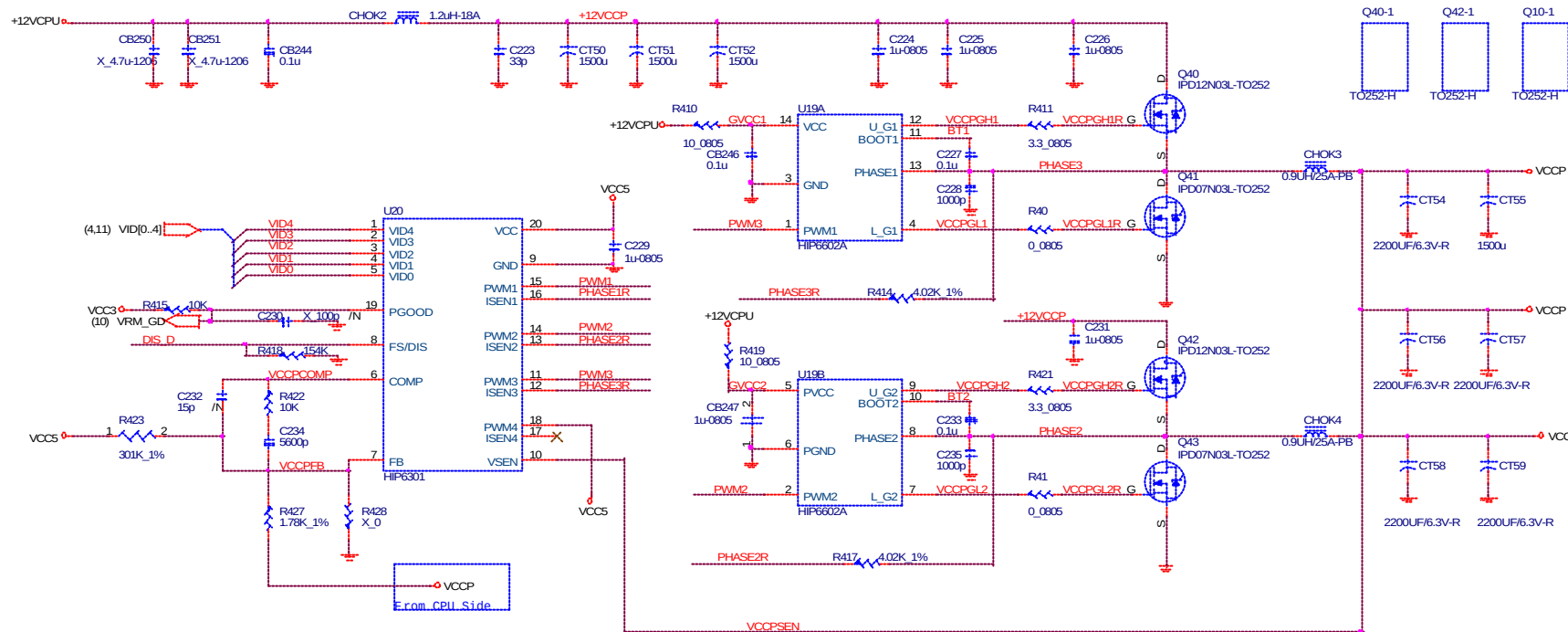
FWH write protect



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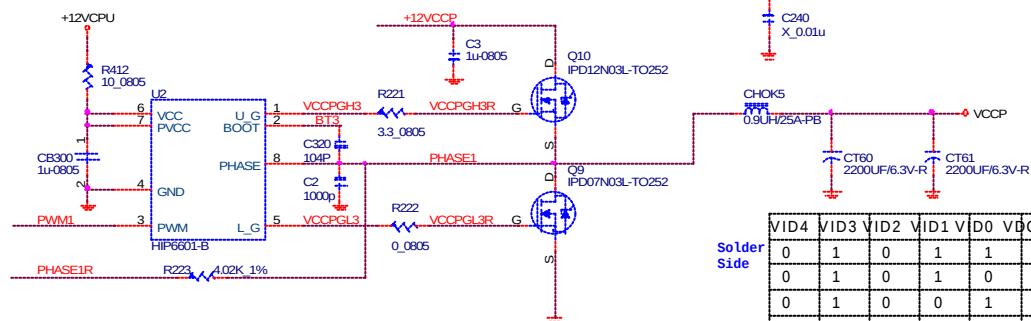
- * AC'97 Trace width : 5 mils
- * AC'97 Trace Spacing : 5 mils
- * Maximum trace length < 8"
- * Length(longest)-Length(shortest)<150mils

Title	FWH	Rev
Document Number	MS-6555	3.0
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HIP6301 -- VRM 9.0/9.2

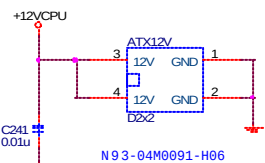
VID4	VID3	VID2	VID1	V	D0	VDC(V)
1	1	1	1	1	1	OFF
1	1	1	1	0	0	1.100
1	1	1	0	1	1	1.125
1	1	1	0	0	0	1.150
1	1	0	1	1	1	1.175
1	1	0	1	0	0	1.200
1	1	0	0	1	1	1.225
1	1	0	0	0	0	1.250
1	0	1	1	1	1	1.275
1	0	1	1	0	0	1.300
0	1	1	1	1	1	1.325
0	1	1	1	0	0	1.350
0	1	0	1	1	1	1.375
0	1	0	1	0	0	1.400
0	1	0	0	1	1	1.425
0	1	0	0	0	0	1.450
0	1	1	1	1	1	1.475
0	1	1	1	0	0	1.500
0	1	1	0	1	1	1.525
0	1	1	0	0	0	1.550



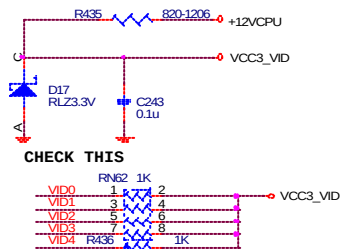
NOTE: INSIDE ON CPU SOCKET.

VID4	VID3	VID2	VID1	V	D0	VDC(V)
0	1	0	1	1	1	1.575
0	1	0	1	0	0	1.600
0	1	0	0	1	1	1.625
0	1	0	0	0	0	1.650
0	0	1	1	1	1	1.675
0	0	1	1	0	0	1.700
0	0	1	0	1	1	1.725
0	0	1	0	0	0	1.750
0	0	0	1	1	1	1.775
0	0	0	1	0	0	1.800

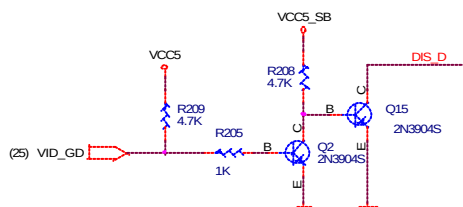
ATX12V POWER CONNECTOR



VID PULL-UP RESISTORS

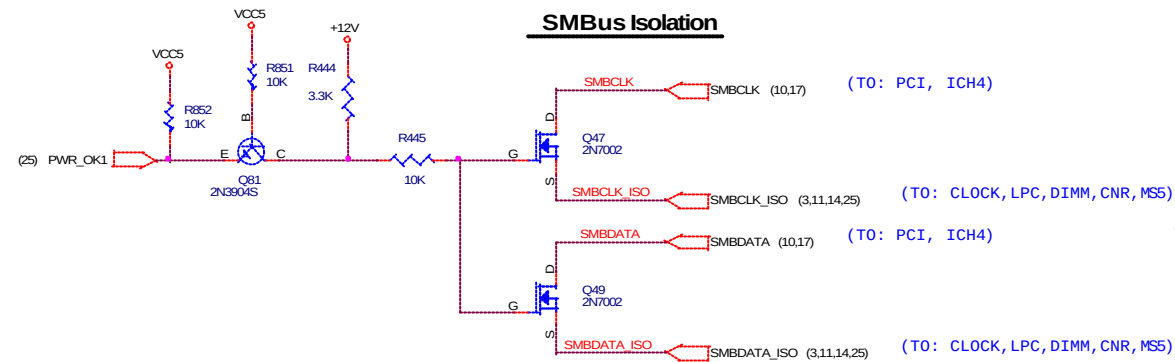


PWM GOOD



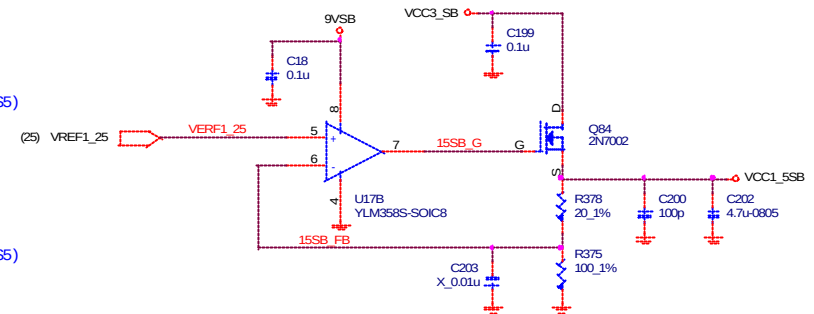
Micro Star Restricted Secret

Title	VRM 9.0	Rev	3.0
Document Number	MS-6555		
MICRO-STAR INT'L CO., LTD.	Last Revision Date: Monday, August 19, 2002		
No. 69 Li-De St, Jung-He City, Taipei Hsien, Taiwan	Sheet	22	of 31
http://www.msi.com.tw			

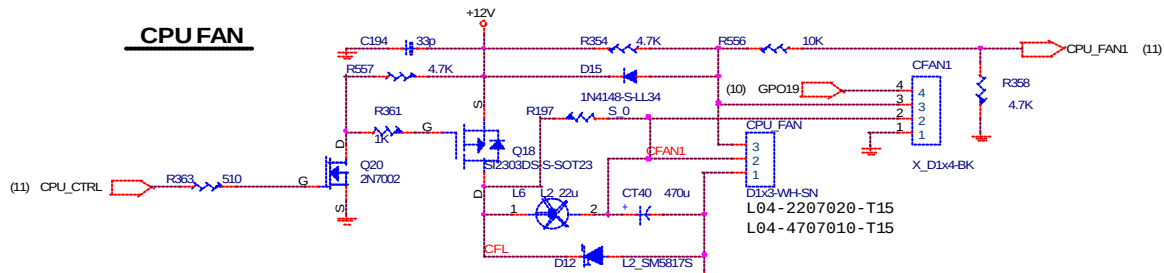


1.5V STANDBY POWER TRANSLATOR

(40mils trace/20 mils space)

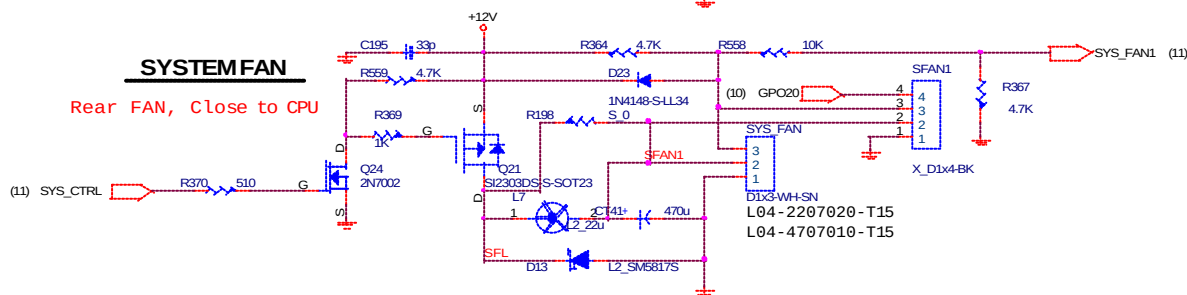


CPU FAN

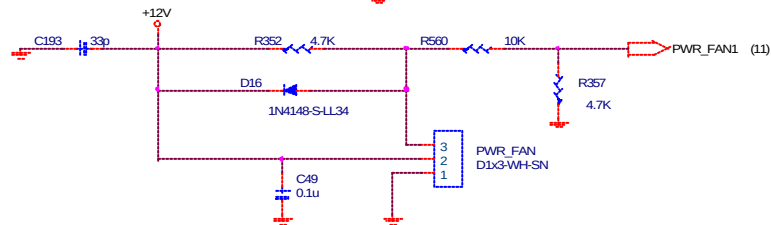


SYSTEM FAN

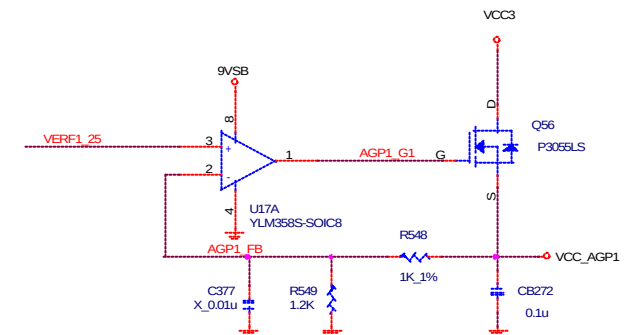
Rear FAN, Close to CPU



POWER FAN

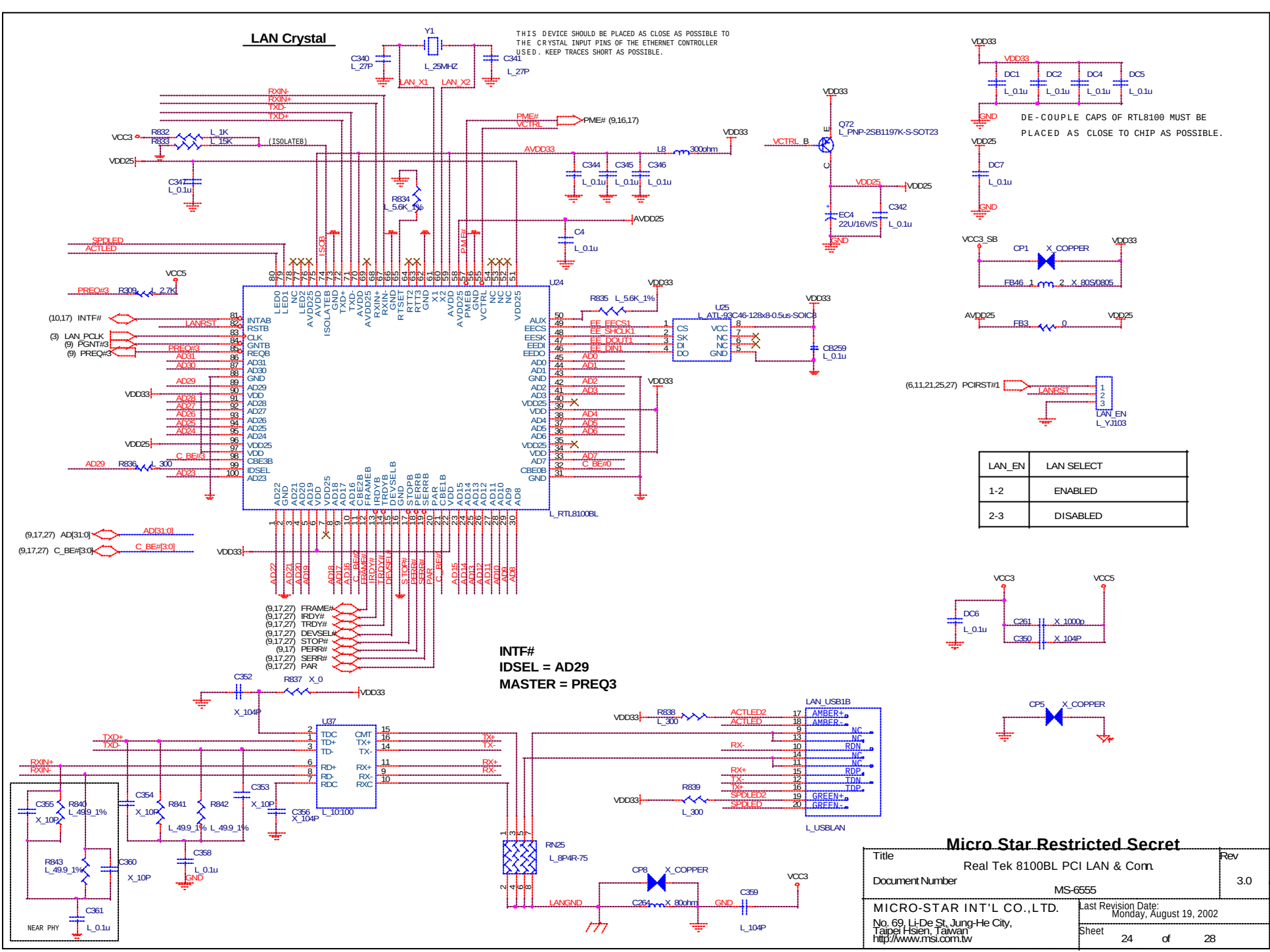
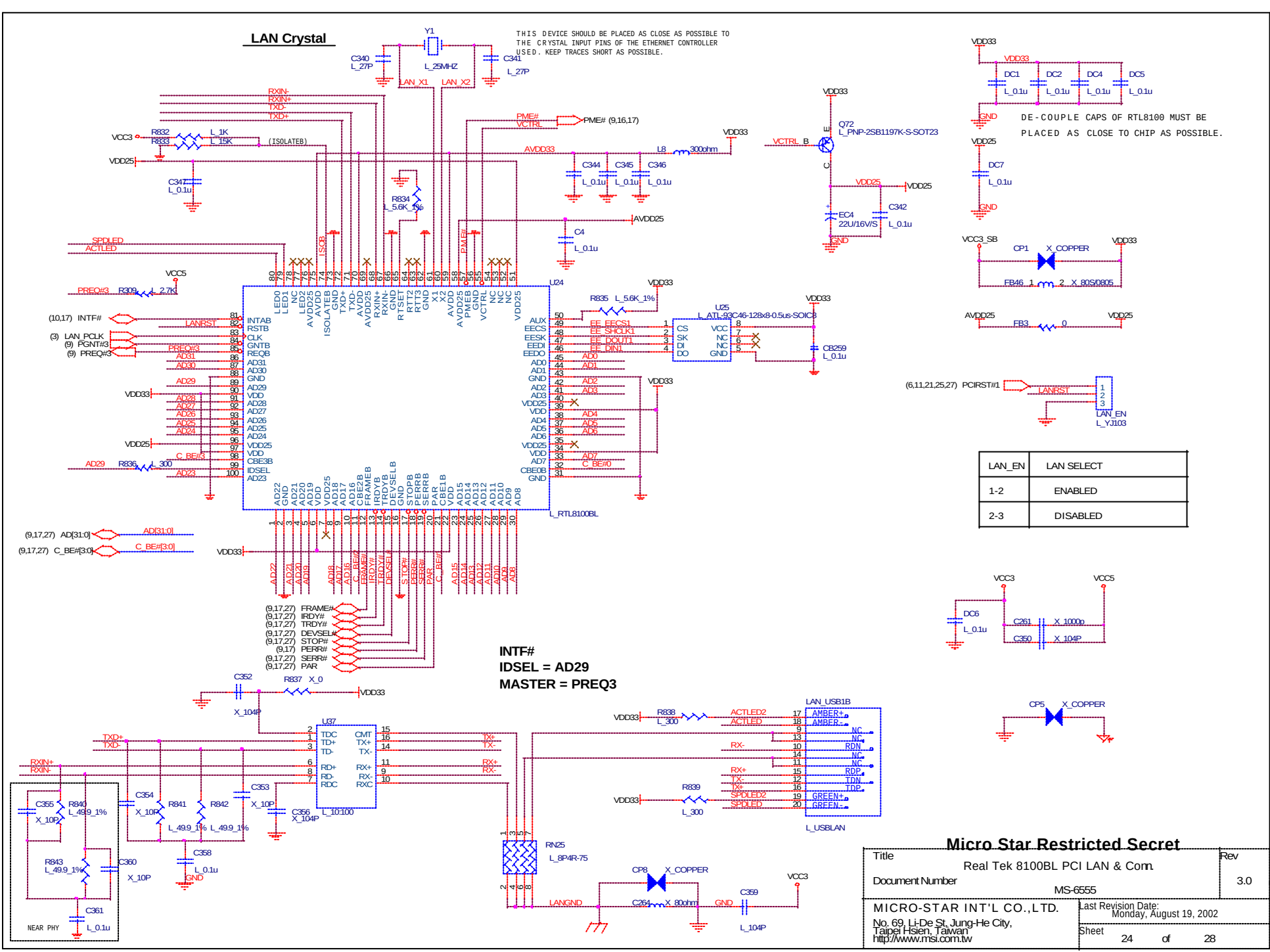


AGP4X & GMCH 1.5V POWER TRANSLATOR



Micro Star Restricted Secret

Title	SMBUS Isolation & FAN Conn.	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO.,LTD.		Last Revision Date:
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Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	OV
MEM_STR	Main	Standby	OV

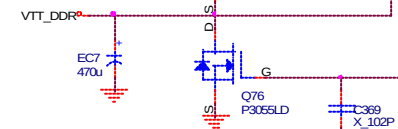
SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

5VUSB USE 2 MOSFET
 **S50# pin function(Hi level = 5V)
 same as 5VUSB(Hi level = 12V)

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
 OUTPUT 1 AND 2 FOR GPIO FUNCTION

DDR VTT Power

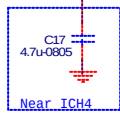
1.25V/2.1A



SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

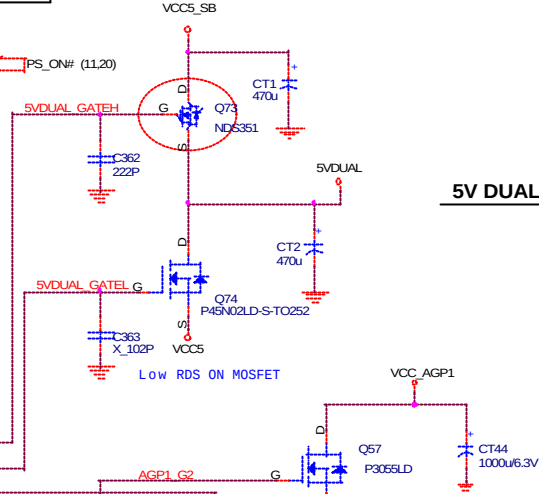
FOR 3VSB OR 3VSTR
 SETTING BY SEL1

Pin 15,19,22,32 Must
 reserve capacitor.



** SETTING 3VSTR THEN VRAM_2.5
 BECOME TO 1.25 VREF

5V DUAL Power



CHARGE PUMP VOLTAGE OUTPUT

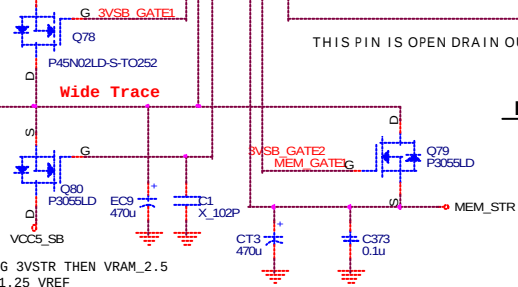
VCC_VID / VID_GOOD

Place MOSFET near CPU

THIS PIN IS OPEN DRAIN OUTPUT

DDR 2.5V Power

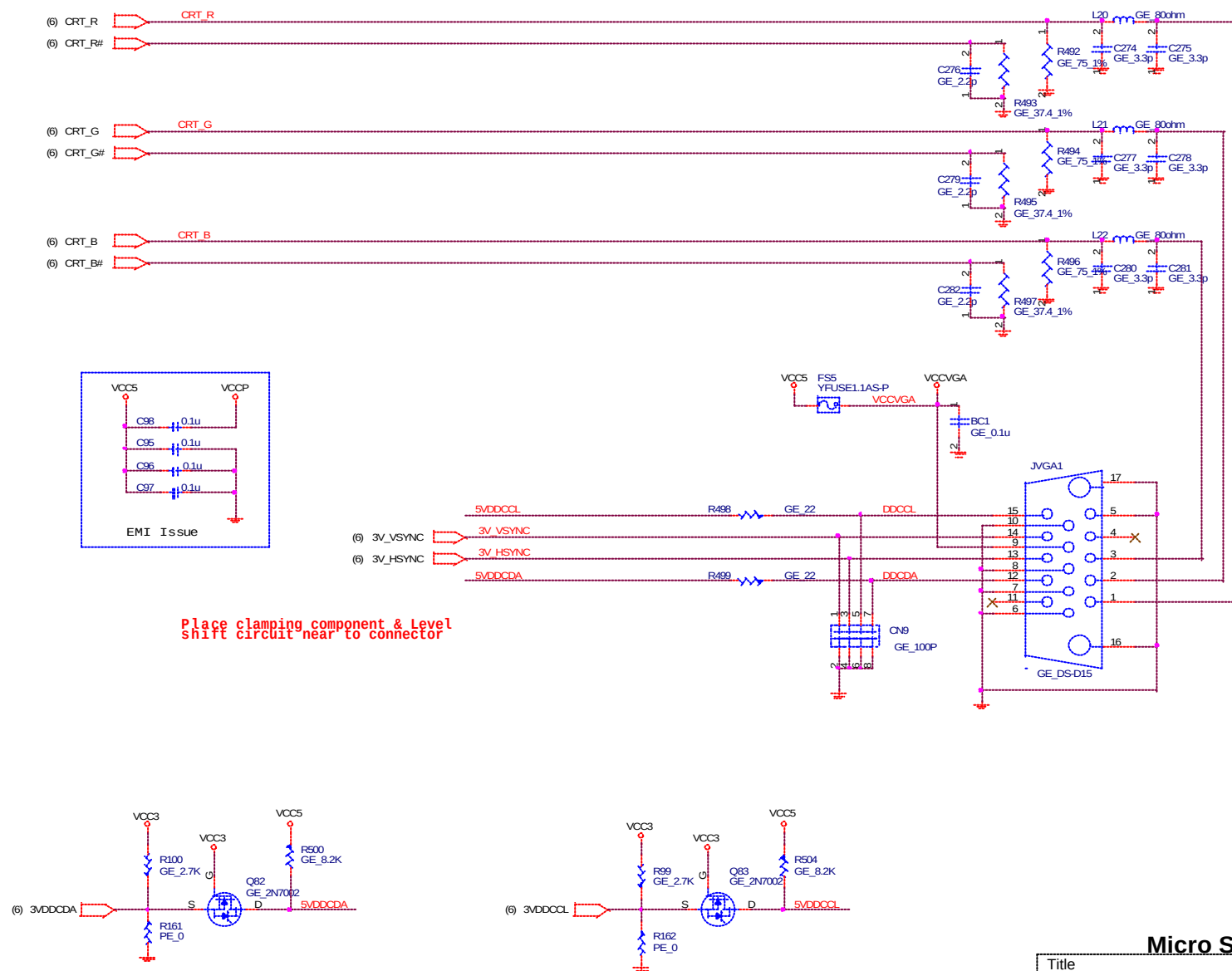
2.5V/2.8A+5.92A



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Title	W83302D(MS-5) ACPI Controller	Rev	3.0
Document Number	MS-6555		
MICRO-STAR INT'L CO.,LTD.	Last Revision Date: Monday, August 19, 2002		
No. 69 Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Sheet	25	of 31

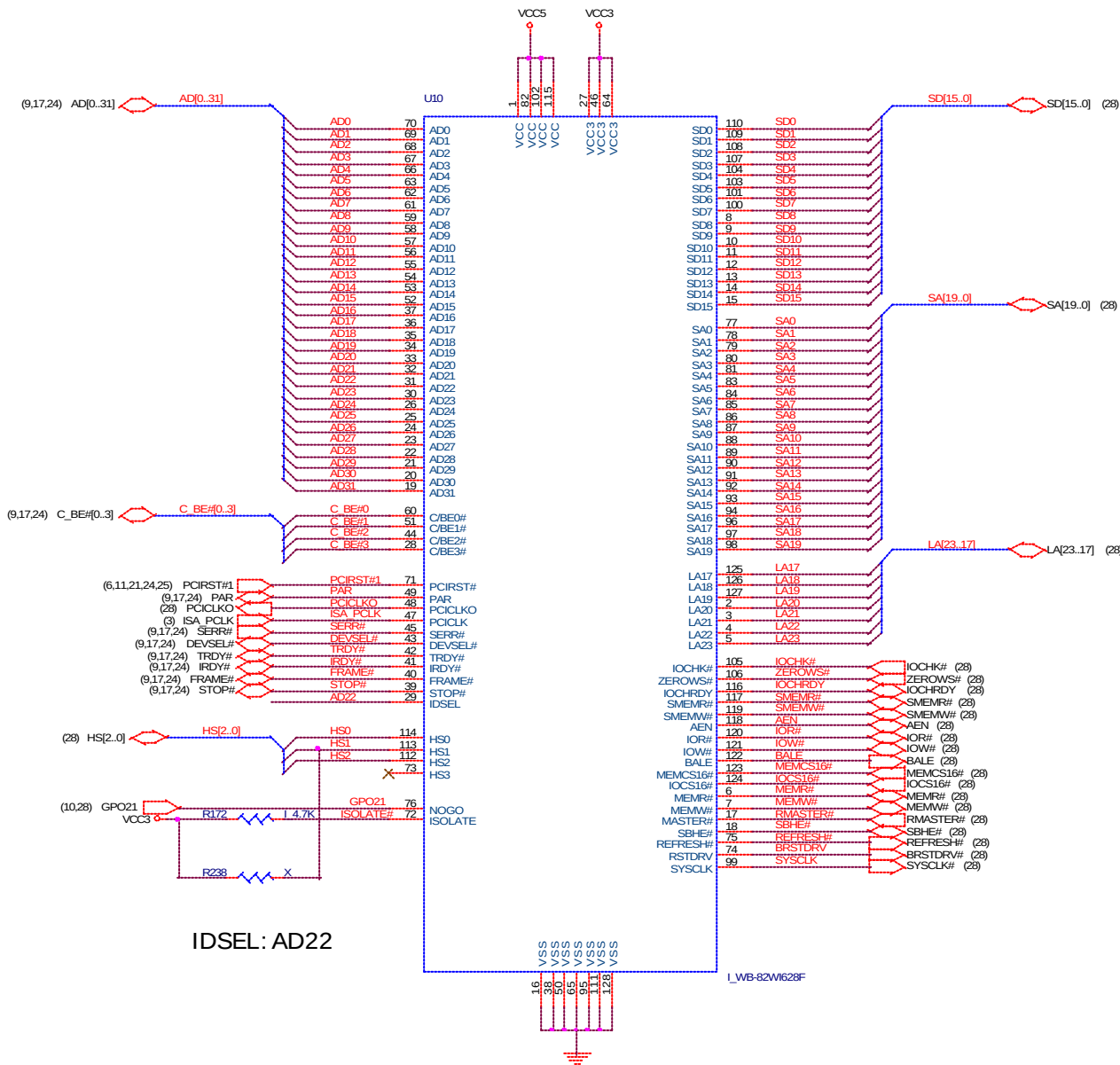
Video Connector



Micro Star Restricted Secret

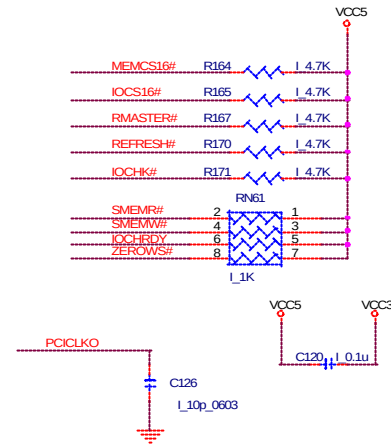
Title		Rev
VGA Conn		
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 19, 2002 Sheet 26 of 31

PCI To ISA Bridge, Part 1



IDSEL: AD22

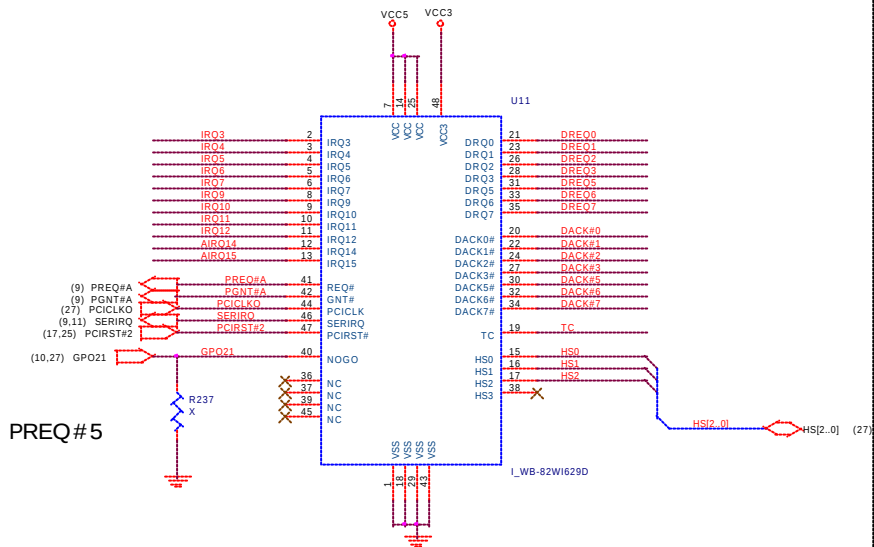
PCI to ISA Bridge Pull Up / Low



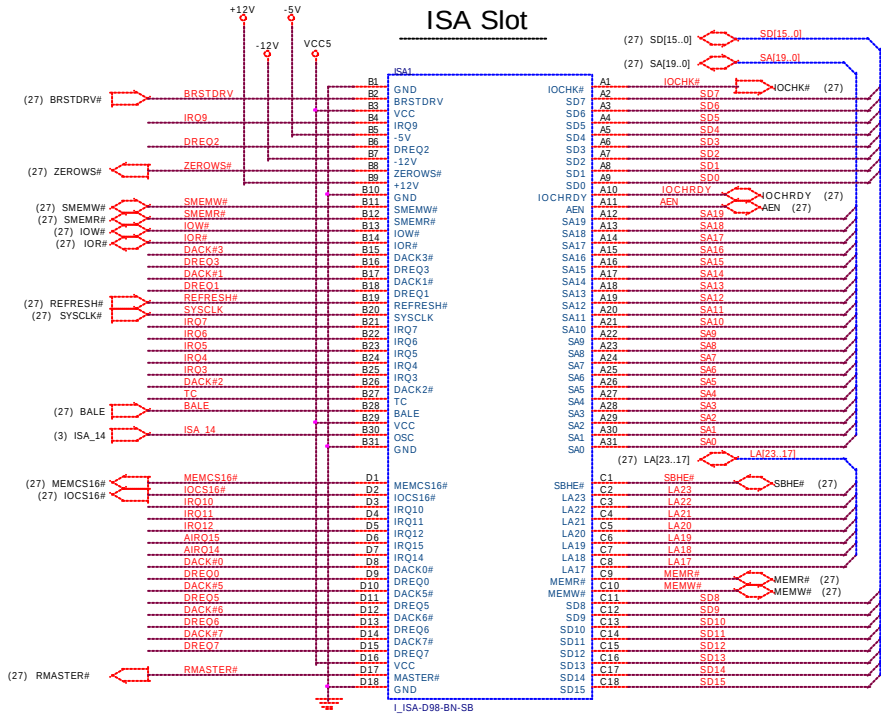
Micro Star Restricted Secret

Title	VGA Com	Rev
Document Number	MS-6555	3.0
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 19, 2002
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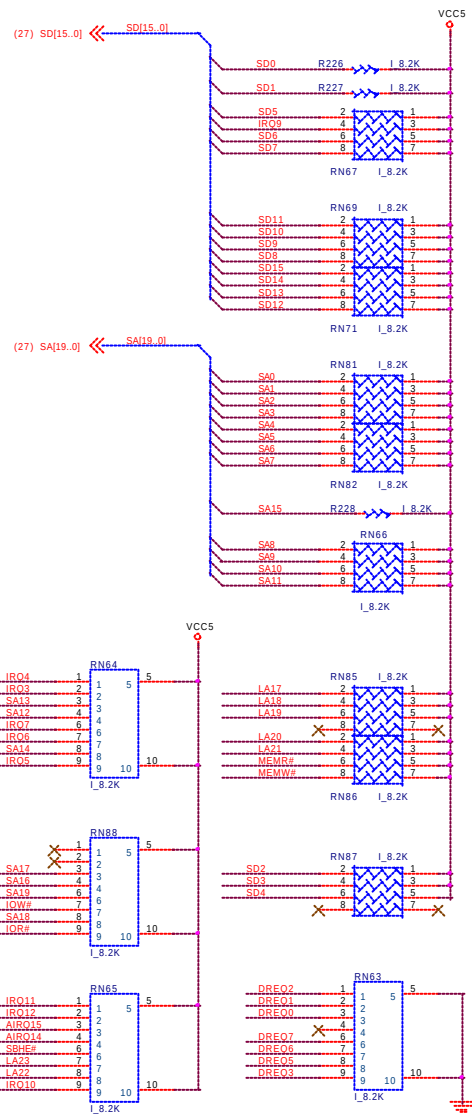
PCI To ISA Bridge, Part 2



ISA Slot

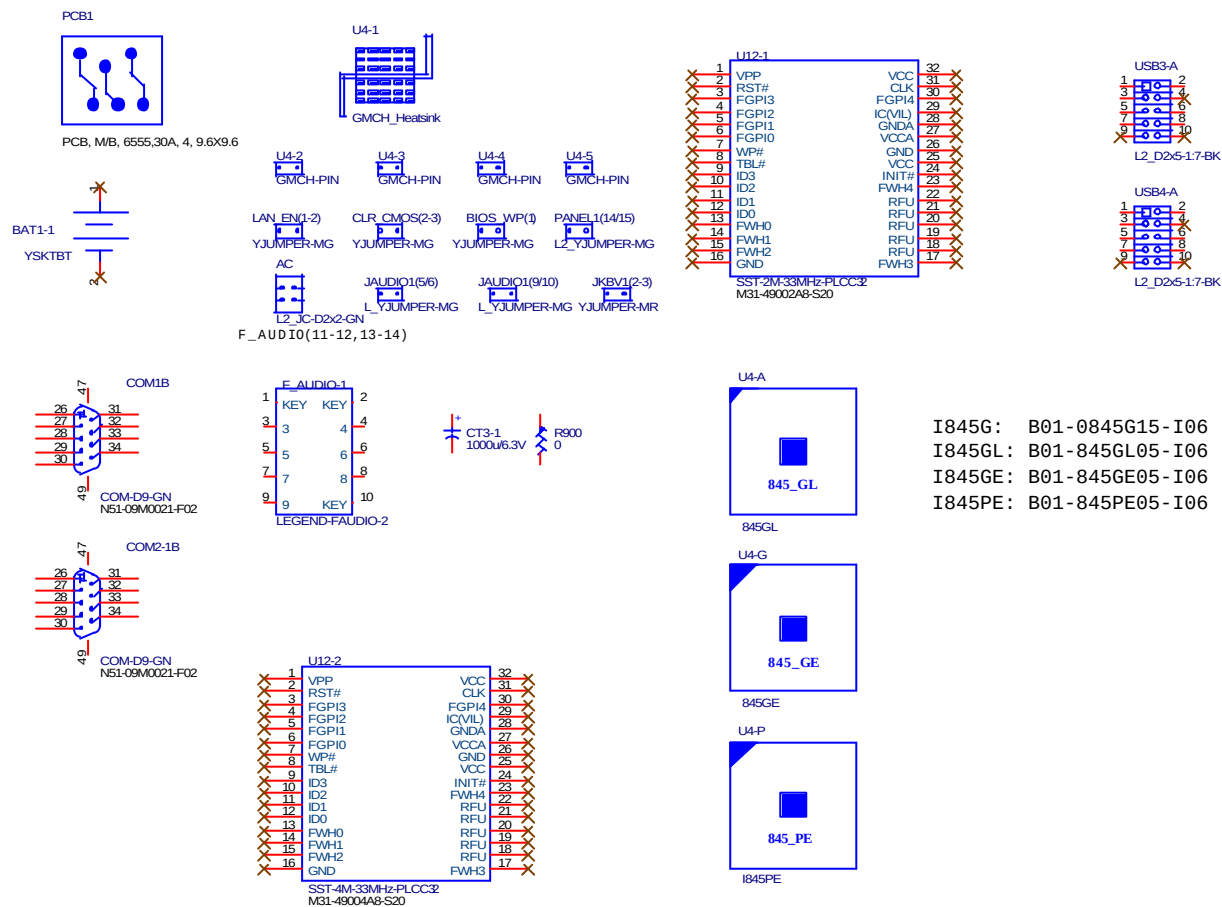


PCI to ISA Bridge Pull Up / Low



~~Micro Star Restricted Secret~~

Title		VGA Conn	Rev
Document Number		MS-6555	3.0
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei, Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 19, 2002	
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Pin Header Key Protect

JFP1 Pin 10
 PANEL1 Pin 2,9,11
 F_AUDIO Pin 8,16
 JAUDIO1 Pin 8
 USB3 Pin 4
 USB4 Pin 4
 USB1 Pin 9
 USB2 Pin 9
 IR1 Pin 2
 COM2 Pin 10

I845G: B01-0845G15-I06
 I845GL: B01-845GL05-I06
 I845GE: B01-845GE05-I06
 I845PE: B01-845PE05-I06

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Title	Manual Parts	Rev
Document Number	MS-6555	2.0
MICRO-STAR INT'L CO.,LTD. No. 69 Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, August 19, 2002
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General SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifunton pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifunction pin)
GPIO 18*	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	No Connected
GPIO 25	I/O	No Connected
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

* GPIO18 will toggle at 1Hz frequency.

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17	PCICLK1	11 (PCI4)
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18	PCICLK2	12 (PCI5)
PCI LAN	INTG# INTF#	AD29	LAN_PCLK	17 (PCI9)

*ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

Micro Star Restricted Secret

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