Besides the H-flag/halt function shown in figure 2-7, the SC/MP chip is readily adaptable to other control circuits. One of these is shown in figure 2-8; here, single-cycle/single-instruction operation is implemented by two flip-flops, two switches, and some simple logic. Switch S1 is set to the desired operating mode and switch S2 is momentarily closed to the NO contact. These events cause the CONT input to go high and the NHOLD input to go low; thus, an instruction is fetched and executed if S1 is set to SINGLE INSTRUCTION, or a fetch-and-wait operation occurs if S1 is set to SINGLE CYCLE. At address-strobe (NADS) time, the flip-flops are cleared for the beginning of a new operation.

At the conclusion of the address strobe, the processor is ready to begin a data-input (read) cycle or a data-output (write) operation. As shown in figure 2-5, the read and write functions are synchronized by the read (NRDS) and write (NWDS) strobes. When the read strobe is low, data are gated from the data bus into the processor; when the write strobe is low, data transferred from the processor to the data bus are guaranteed to be valid. For a given input/output cycle, either the read or the write strobe is active (not both).

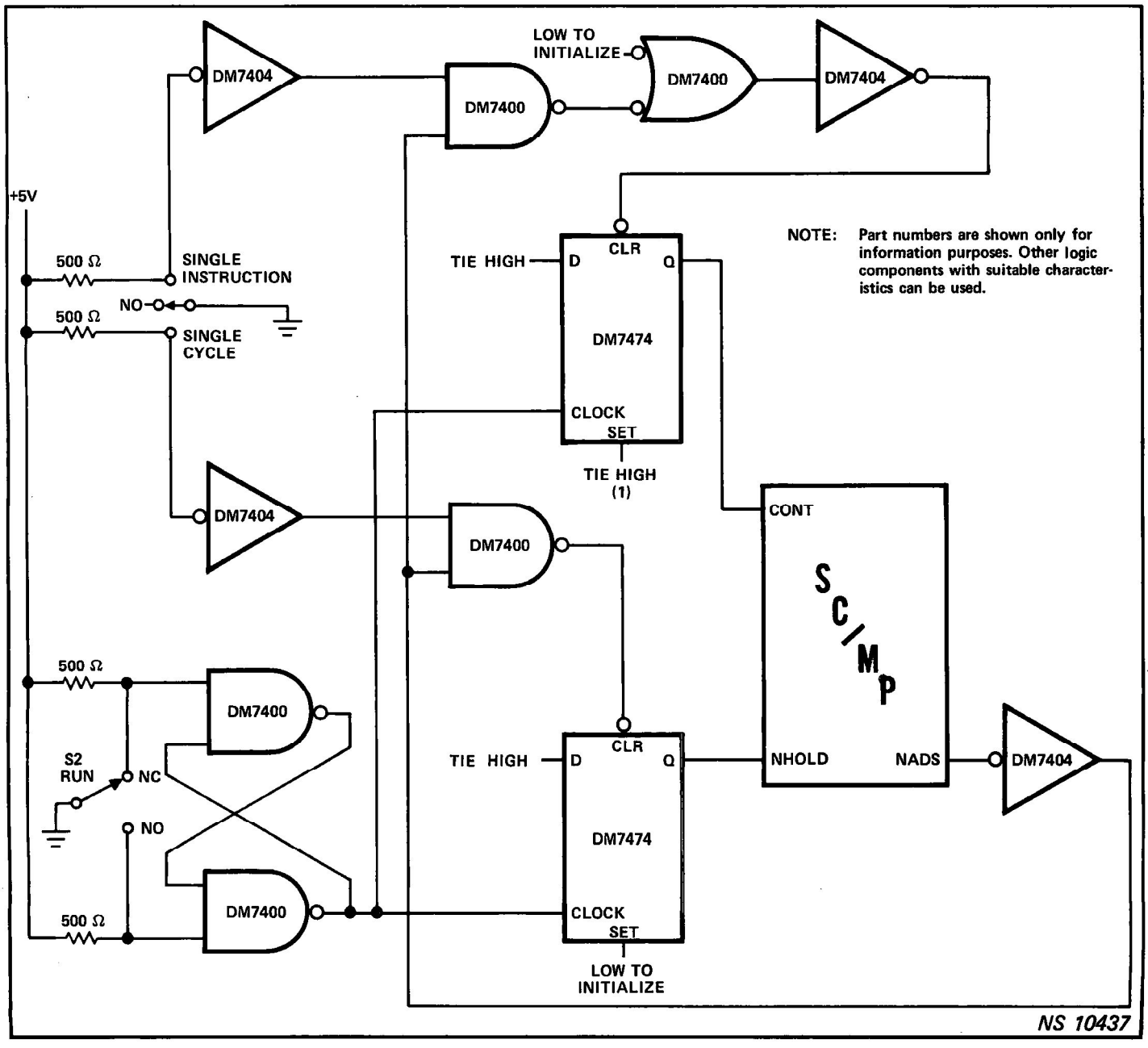

Figure 2-8. Circuit Detail To Implement Single-Cycle/Single-Instruction Control