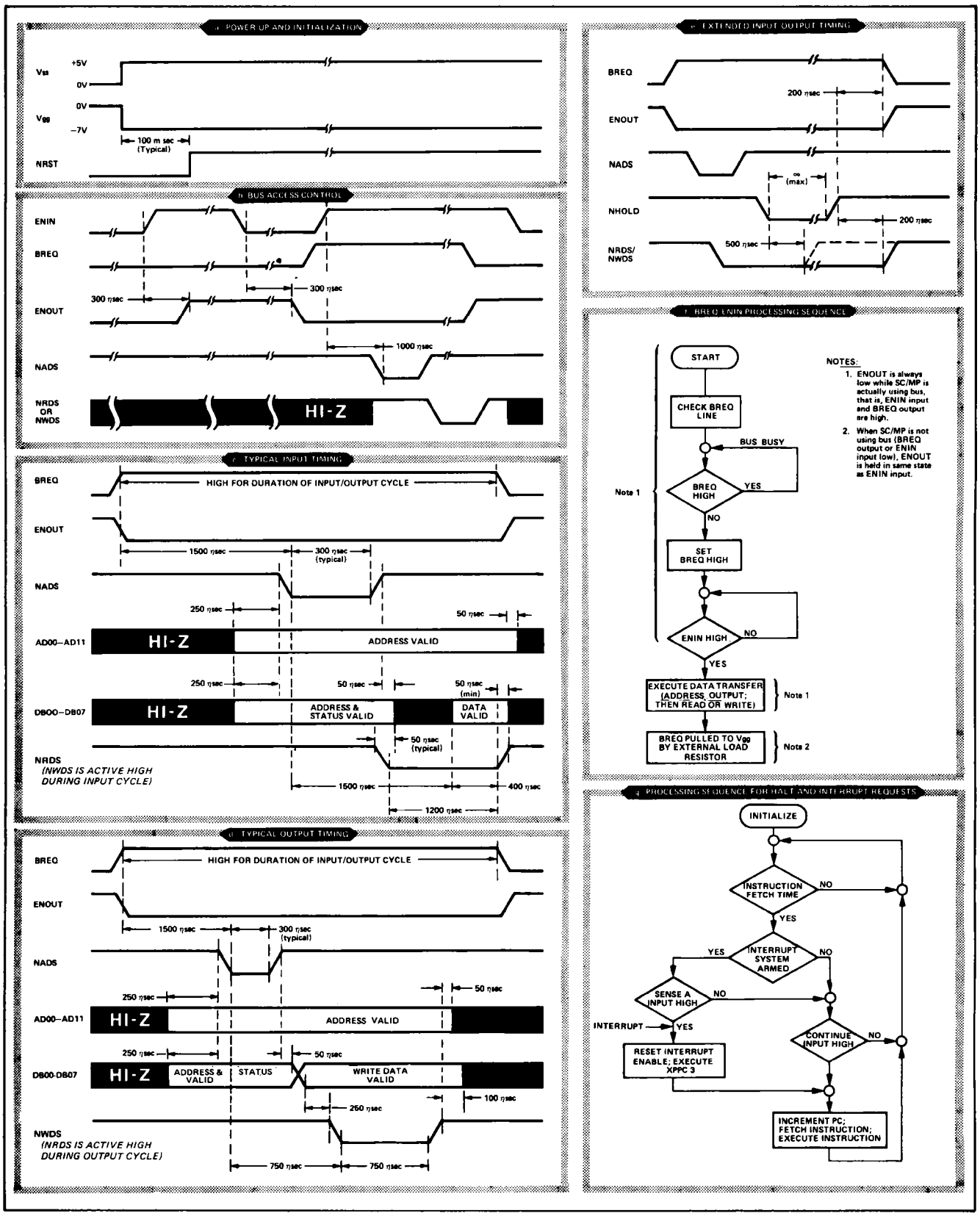

Figure 1–4. SC/MP Timing (Based on 1-MHz Crystal) and Processing Sequences

Table 1-1. Description of SC/MP Pinouts

PIN	Basic Function	Design Considerations	PIN	Basic Function	Design Considerations
X1 37 X2 38	Timing	Connect capacitor between these pins for applications where timing is not critical; use crystal where timing is critical. (Refer to Appendix A for component characterization and the use of an external clock.)	NRST 7	Negative Reset	When this input is set low, in-process operations are aborted.
			NHOLD 6	Wait	In conjunction with CONT, the NHOLD input can be used to implement single cycle/single-instruction control of SC/MP – refer to figure 1-4e for extended input/output timing.
V_{SS} 20	Power	V_{SS} = +5V (±5%)			
V_{GG} 40		V_{GG} = –7V (±5%)			
Sense A 17 Sense B 18	External sensing and software-controlled interrupt	These TTL-level inputs are connected directly to bit positions 4 and 5 of the status register. Both bits can be copied from the status register to the accumulator but neither bit can be written into from the accumulator, that is, they are "read only" inputs. With the interrupt armed (bit 3 of status register set high), the Sense A pin becomes the interrupt input – see figure 1-4g for processing sequence of interrupt request and Appendix C for implementation detail of the interrupt system.	SIN 23 SOUT 24	Serial Input/Output	When the SIO instruction is executed, the MSB of the input data is shifted into the MSB of the extension register, and the LSB is shifted from the E-Register to an output latch, that is, the contents of the register can be changed without affecting the state of the output latch.
			NADS 39	Negative Address Strobe	When low, indicates valid address and status outputs are present on the system buses. The NADS leading edge of the strobe can be used to externally latch input/output status and the four MSB of the 16-bit address; refer to figures 1-4c, 1-4d, and 1-4e for I/O timing of NADS.
Flag 0 19 Flag 1 21 Flag 2 22	External control of peripherals	Each flag output is TTL-compatible and can drive a 1.6-milliampere load. The flags are software-controlled and can be set or pulsed in a single or multiple sequence.			
			NRDS 2	Negative Read Strobe	A Tri-State output that, when low, indicates SC/MP is ready to accept data from the 8-bit input/output bus; as shown in figure 1-4c, data are input on the trailing edge of this strobe.
BREQ 5 ENIN 3 ENOUT 4	Bus-Access, DMA, and Multiprocessor Control	In simple stand-alone applications, BREQ can be connected to V_{GG} through a 6.8 kilohm resistor, ENOUT can be ignored, and ENIN can be connected to V_{SS} so that the SC/MP microprocessor has access to system buses whenever the BREQ pin is high. In systems that require bus-sharing, the common bus-request line is continually tested by each microprocessor; when the request line is low, system buses can be accessed, and if BREQ and ENIN are set high, bus access is granted.	NWDS 1	Negative Write Strobe	A Tri-State output that, when low, indicates output data from SC/MP is valid on 8-bit input/output bus; refer to figure 1-4d for output timing.
			DB 00-07 16...9	Input/Output data	At NADS time, I/O status and 4-MSB of 16-bit address are output from SC/MP; at NRDS time, data are input to SC/MP and, at NWDS time, data are output from SC/MP. Each pin is bidirectional and Tri-State.
CONT 8	Start/Stop	Permits suspension of operations without loss of internal status. Can be used with 'HALT' flag to implement a programmed halt; also, can be used with NHOLD (Wait) signal to implement single-cycle/single-instruction control of microprocessor.	AD 00–11 25 ... 36	Latched Address	At NADS time, the 12-bit latched address is valid and, as shown in figures 1-4c and 1-4d, a read *or* write function then is implemented.

*Refer to SC/MP data sheet for minimum/maximum values.