integrated DTL circuits

volume 7

Type No.	Description and Construction		Propagation Delay (Typ.) (ns)	Fan Out (25°C)	Noise Immunity at 25°C (Typ.) (mV)	Noise Immunity at 125°C (min.) (mV)	Supply Voltage (V)	Operating Temperature (°C) (min.)	Operating Temperature (°C) (max.)	P_{tot} Average (mW)
OMY100 OMY120	DTL NOR/NAND gate with 3 inputs	AT	23	6 4	950	400	±6·0	−55 0	+125 + 75	18
OMY101 OMY121	DTL symmetrical (bistable circuit with set and reset facility)	AT		5	950	400	±6·0	−55 0	+125 + 75	40
OMY102 OMY122	Resistor-diode-capacitor logic steering circuit for OMY101/121	AT	Max. Operating Frequency 2 (MHz)				±6·0	−55 0	+125 + 75	3·5
OMY123	Inverting buffer amplifier	AT	50	20	900	400	±6·0	0	+ 75	100
OMY104 OMY124	DTL NAND/NOR dual logic gate	AT	23	6 4	950	400	±6·0	−55 0	+125 + 75	36
OMY105 OMY125	5 diodes expander unit	AT						−55 0	+125 + 75	250
OMY106 OMY126	JK Flip-flop with direct set and reset terminals bidirectional circuit output	AT	Counting rate min. 10 (MHz)	3 3		250	+6·0	−55 0	+125 + 75	55

Type No.	Description and Construction		Propagation Delay (Typ.) (ns)	Fan Out (25°C)	Noise Immunity at 25°C (Typ.) (V)	Supply Voltage (V)	Operating Temperature Range (°C)	Av. Power Dissipation (per Gate) 25°C (50% Duty Cycle) (mW)
FCH101 FCH102	8 input DTL NAND/NOR gate with nodes	AU AV	30	7 11	1·1	+6·0	0 to + 75 −55 to +125	12 9·5
FCH111 FCH112	8 input DTL NAND/NOR gate with nodes and collector resistors	AU AV	19	7 11	1·1	+6·0	0 to + 75 −55 to +125	21 15
FCH121 FCH122	Dual 4-input DTL NAND/NOR gate with nodes	AU AV	30	7 11	1·1	+6·0	0 to + 75 −55 to +125	12 9·5
FCH131 FCH132	Dual 4-input DTL NAND/NOR gate with nodes and collector resistors	AU AV	19	7 11	1·1	+6·0	0 to + 75 −55 to +125	21 15
FCH141 FCH142	Triple 3-input DTL NAND/NOR gate with node input on gate 1	AU AV	30	7 11	1·1	+6·0	0 to + 75 −55 to +125	12 9·5
FCH151 FCH152	Triple 3-input DTL NAND/NOR gate	AU AV	30	7 11	1·1	+6·0	0 to + 75 −55 to +125	12 9·5
FCH161 FCH162	Triple 3-input DTL NAND/NOR gate with collector resistors and node on gate 1	AU AV	19	7 11	1·1	+6·0	0 to + 75 −55 to +125	21 15
FCH171 FCH172	Triple 3-input DTL NAND/NOR gate with collector resistors	AU AV	19	7 11	1·1	+6·0	0 to + 75 −55 to +125	21 15
FCH181 FCH182	Quadruple 2-input DTL NAND/NOR gate	AU AV	30	7 11	1·1	+6·0	0 to + 75 −55 to +125	12 9·5