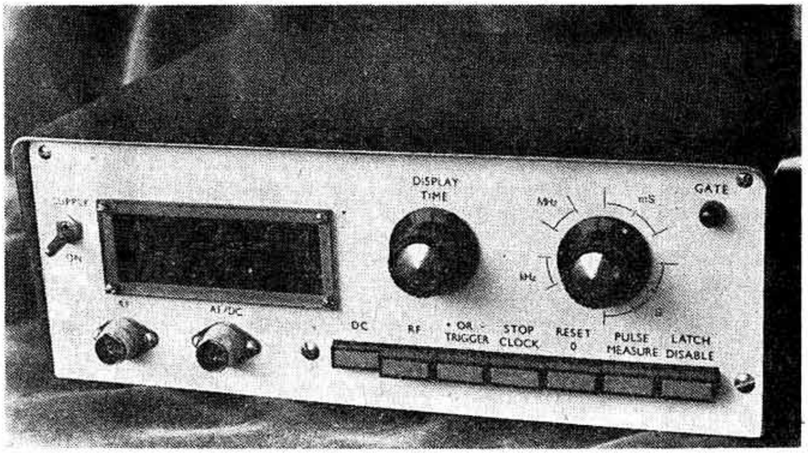
A digital frequency counter and timer

(direct read-out at 150MHz)



by G. F. FIRTH, G3MFJ,* and D. M. PRATT, G3KEP†

THE instrument to be described is a digital frequency counter and timer which was designed to measure frequency up to 150MHz and periods of time from 1μs upwards. No apology is offered for submitting details of another counter/timer as it is felt that other published designs do not fully exploit all the facilities which such an instrument is capable of providing. Using new components the counter/timer can be built for approximately £35, which compares favourably with commercially available counters of similar specification currently selling for well over £100.

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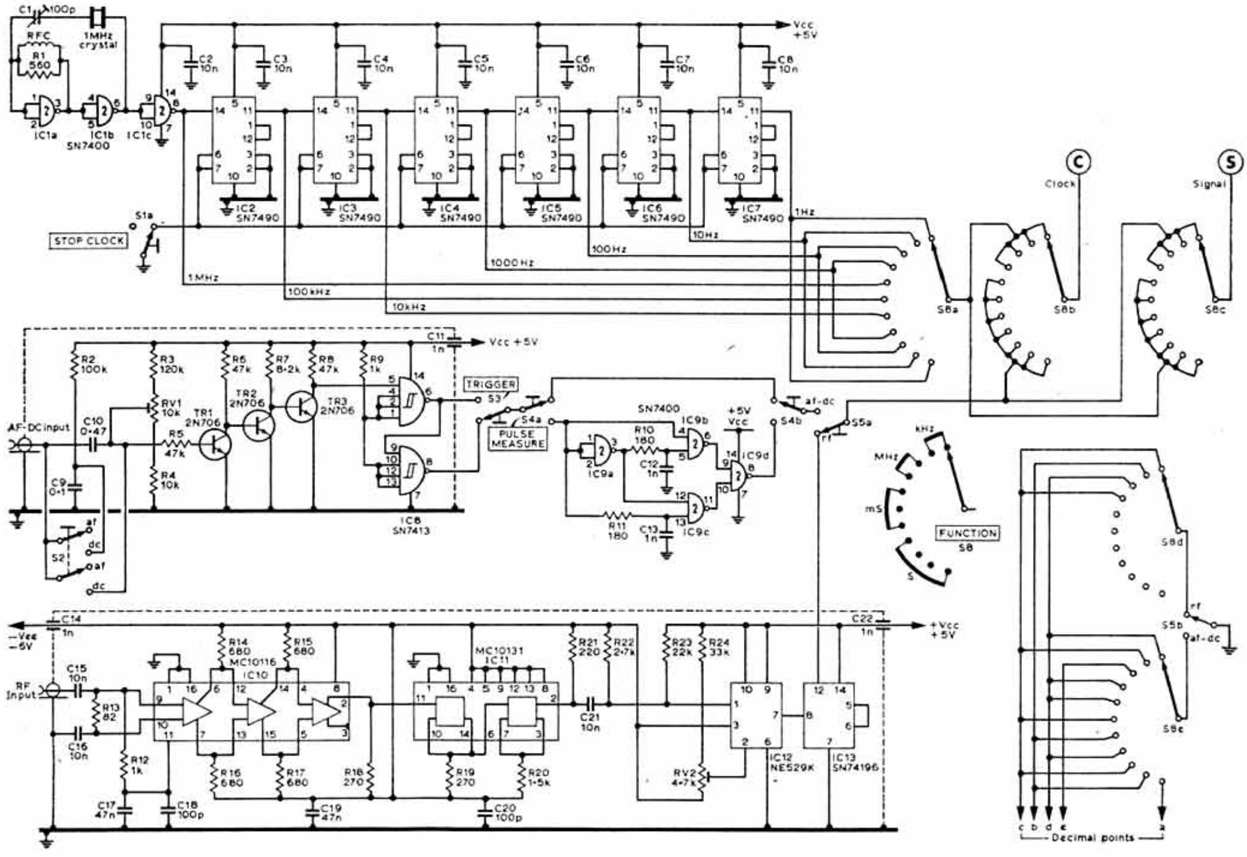


Fig 1 (above and right). Circuit diagram of the counter/timer

Specification

The instrument has two principal functions—(a) a frequency counter, and (b) a period timer. The facilities of each function are as follows:

(a) **Frequency counter**

(i) **af/dc input.** This input will accept frequencies within the range dc to 1·5MHz, resolution being to 1Hz. The average sensitivity on this range is approximately 25mV.

(ii) **rf input.** Frequencies from 200kHz to over 150MHz may be measured using this input, the upper frequency limit being determined by the individual characteristics of the ic used. Resolution is to 10Hz and the average sensitivity over the range is approximately 20mV.

Both the above input circuits give a steady, non-blinking display.

(b) **Period timer**

(i) Periods from 1μs to thousands of seconds can be measured, the resolution being determined by the five digits of display.

(ii) The timer may be started or stopped with a positive- or a negative-going pulse. The start and stop pulses may be of the same or of opposite polarities.

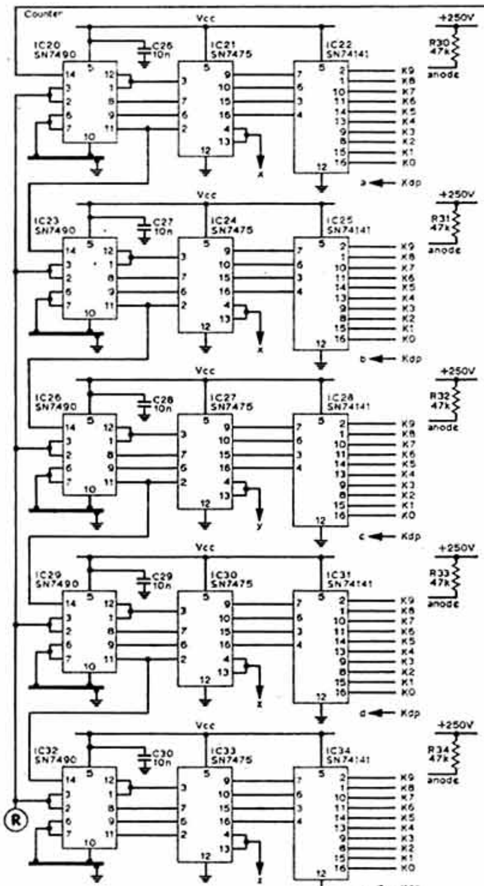
(iii) Using the memory facility, the display of time can be held for inspection while the unit continues to time. The display may be brought up to date with the time when desired.

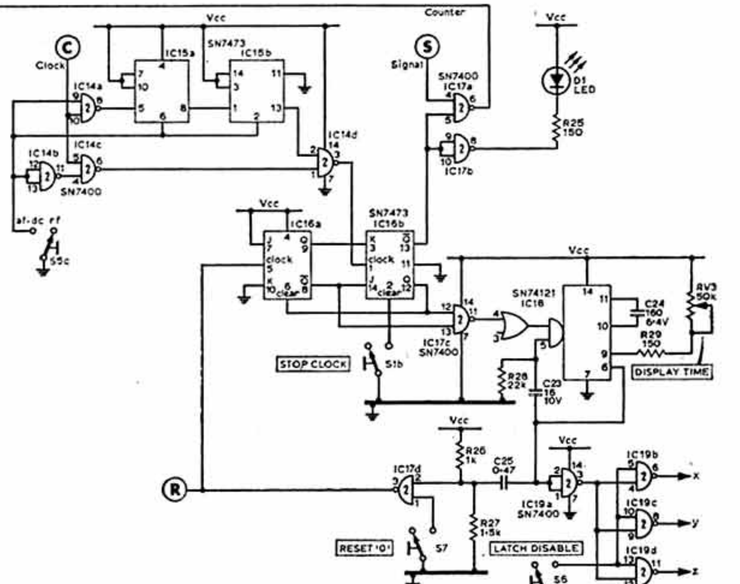
(iv) Pulses can be counted with the unit in its frequency counter mode with the clock stopped, ie the number of pulses fed to the input socket is counted rather than the duration or frequency of them.

The accuracy of the instrument will depend upon the quartz crystal standard. As a frequency counter a short term accuracy of 1 part in 10^7 should be easily obtainable. However, to this must be added a further inaccuracy of ± 1 digit due to the internal clock not being synchronized with the frequency being measured. This error may be overcome, but the additional circuitry involved was not considered justified.

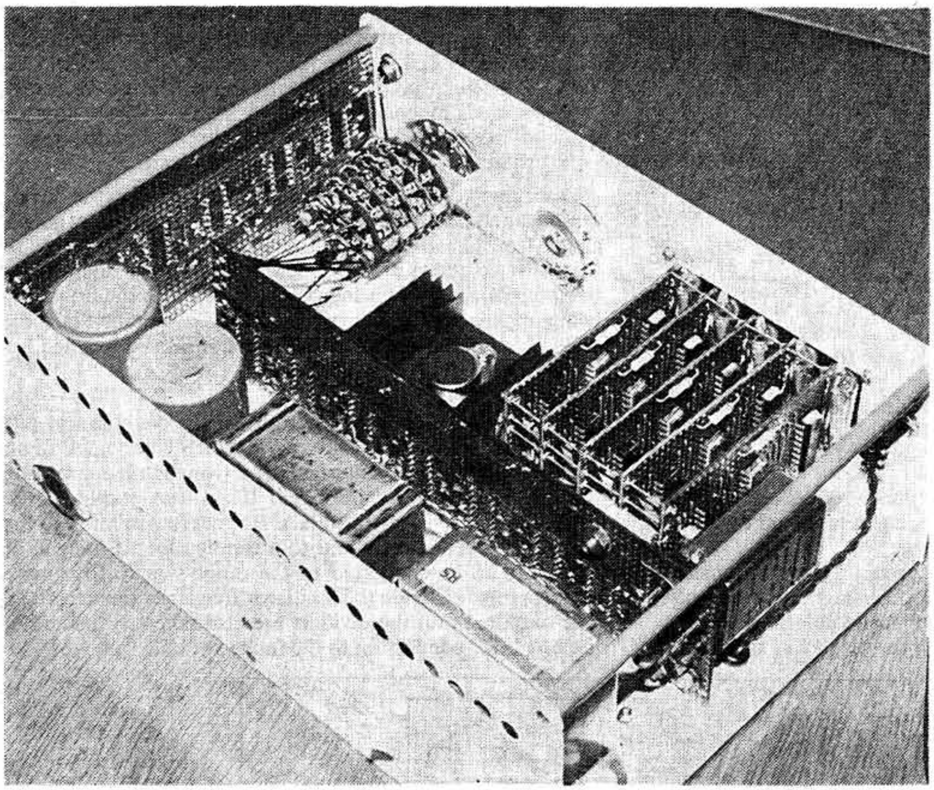
Circuit description

The clock pulse supply is the basis of the counter and this will be considered first. The crystal which is mounted in an oven for stability is connected to an oscillator comprising the two NAND gates IC1a and IC1b. The output of the oscillator is fed via the third NAND gate for isolation to the first decade divider IC2 and to a termination at the end of the board to be connected to the range switch. Five more dividers further divide the oscillator frequency down to 1Hz. The outputs of all the dividers are also taken to the end of the board for connection to the range switch.





The af/dc input circuit consists of a dual Schmitt trigger IC8, the two parts of which are connected in cascade to give two outputs 180° out of phase. The first of the Schmitt triggers is driven from three directly-coupled 2N706 transistors, the first one of these being given a preset bias control. This sets the operating condition for the whole amplifier. The input socket is capacity coupled to the first transistor and provision is made for short circuiting this capacitor C10 for dc control signals. In the dc position a capacitor C9 is connected across the input socket to overcome the effect of



Top view of the counter/timer showing the display boards (right); regulator ic mounted on heatsink, and clock board with crystal oven mounted on it (centre), and main control board (left)

contact bounce at the input signal source. A small additional bias is connected to the first stage via R2 so that a simple "make" contact will control the counter for timing purposes. The two outputs of this circuit are fed via the trigger polarity reversing switch S3 to a pulse doubler circuit IC9 if S4 is operated. The function of this circuit is to provide a positive-going 1μs pulse for every change of state of the input pulse. This allows the counter to time the length of a single input pulse, a facility not often found in other counter designs. IC9a and IC9b together provide a pulse for a positive-going input signal, and IC9a and IC9c do the same for a negative-going input signal. IC9d operates as an OR gate combining the two signals. The output of this circuit is connected to the range switch S8 via the af/dc—rf selector switch S5a. In the rf position of this switch the rf input circuit is connected.

The rf input circuit uses a triple-stage amplifier IC10, the sections of which are connected in cascade. The output is fed to two divide-by-two circuits in IC11 which gives an output of one quarter of the input frequency. These two ICs have a guaranteed minimum operating frequency of 150MHz. In the prototype the counter operated satisfactorily up to 185MHz. As these two ICs use emitter coupled logic (ecl) which requires a negative supply rail V_{ee}, the output is not compatible with ttl and therefore some form of level converter is necessary. As the output frequency will be over 40MHz it was felt that something a little more sophisticated than the usual single transistor was required. The device chosen was a Signetics NE529K, IC12. This is a high-speed comparator with a differential input and a ttl compatible output. The samples checked before the device was finally incorporated all operated to over 70MHz. The output of this is fed into a high-speed ttl decade divider, IC13, a 74196 which will operate to at least 50MHz. This means that the input frequency is divided by 40, and the output frequency will be less than 5MHz, well within the capacity of normal ttl.

The outputs of the clock board are fed to S8a which selects the appropriate clock rate, and the wiper of S8a together with the wiper of S5a are fed to S8b and S8c. These two wafers act as a double-pole changeover switch connecting either the appropriate clock pulse or the input signal to the gate control circuit, the opposite applying to the display. S8c is fed direct to one input of the control gate IC17a, the other input being fed from the control circuit. The output of IC17a is connected to the first digit board, ie the least significant digit.

All the digit boards are identical and each consists of a decade counter IC20, IC23 etc, a quad latch IC21, IC24 etc, and a decoder IC22, IC25 etc. The binary coded decimal (bcd) outputs of the decade counter are fed into the quad latch which acts as a temporary store and holds the last digit while the next one is being counted. The output of the latch is fed to the decoder. In this design cold cathode indicating tubes are used, but if other types of display are required then it is a simple matter to fit the appropriate type of decoder here. The "D" output of each decade counter is also fed to the next digit board input except of course for the last (most significant) digit.

The control circuit operation is as follows. The clock signal from S8b is fed into IC14 and IC15. The function of this circuit is to divide the clock frequency either by four or

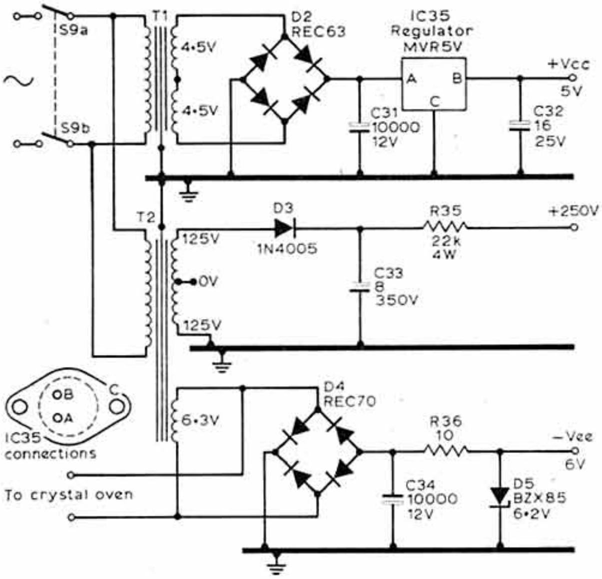
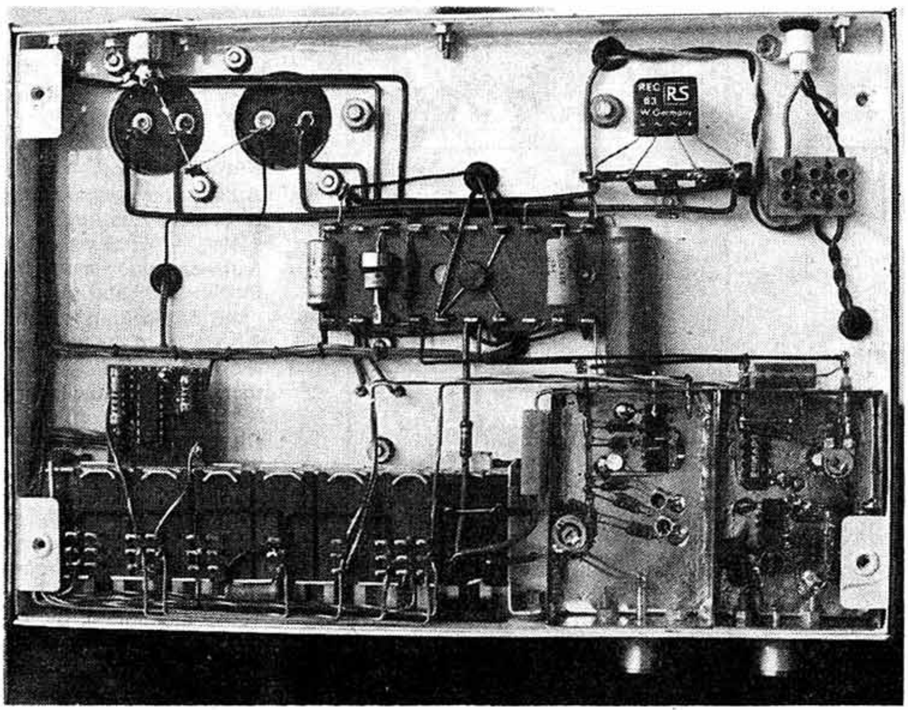


Fig 2. Power supply circuitry

by one. It is divided by four when the rf input circuit is in use, so cancelling out the effect of the divide-by-four section of that circuit. When the af/dc input circuit is in use no division is necessary. The action of this circuit is controlled by S5c. The output of IC14d is fed into the clock input of IC16b, the $\bar{Q}$ output of which controls the control gate. IC16b also controls IC17b, the gate indicator LED driver. The operation of this portion of the circuit is as follows. Assuming that IC16a Q is high and IC16b $\bar{Q}$ is low, the next clock pulse will cause IC16b $\bar{Q}$ to go high thus opening the main control gate. When IC16b $\bar{Q}$ is high IC16b Q will be low clearing IC16a, ie makes IC16a Q low. The next clock pulse will cause IC16b $\bar{Q}$ to go low which will close the main control gate. At this point the output of IC17c will go high and trigger the monostable IC18. The Q output of IC18 will go high so releasing the latch inputs on all the display boards via IC19. After a period determined by the capacitor C24 and RV3 the Q will go low again. The low on IC18 Q through IC19 latches the count on all the displays. After a short delay produced by C25, IC17d will give a short high pulse which will reset all the decade dividers to zero. This also makes IC16b ready for the next clock pulse by making IC16a Q high.

S8d and S8e control the decimal points on the indicator tubes. Two wafers are required and these are selected by S5b which moves the decimal point one place to the right when the rf input is used. The tubes used in the prototype have both left- and right-hand decimal points and the circuit diagram assumes that the right-hand one is used. If the display devices used have only a left-hand decimal point, appropriate rearrangement of S8d and S8e will be necessary.

The power supply uses standard circuitry using two transformers. Transformer T1 has two secondary windings connected in series providing a 9V output which is rectified by D2. Smoothing is achieved with C31, and a fixed-voltage regulator IC35 provides a stabilized 5V positive supply V_{cc}. Transformer T2 has two secondary windings, the first being used after rectification and smoothing to provide 250V for the indicator tubes. A 6·3V winding is used for the crystal oven, and is also rectified to provide a negative supply for the rf input circuit (V_{ee}). A zener diode D5 is used in a simple stabilization circuit. A three-way DIN socket is



Underside view of the instrument. The rf input circuit is in the bottom right-hand corner with the af/dc circuit in the box to its left. The power supply components are mounted on a 10-way tag board in the centre. The small Veroboard panel containing one ic is the pulse measure circuit IC9

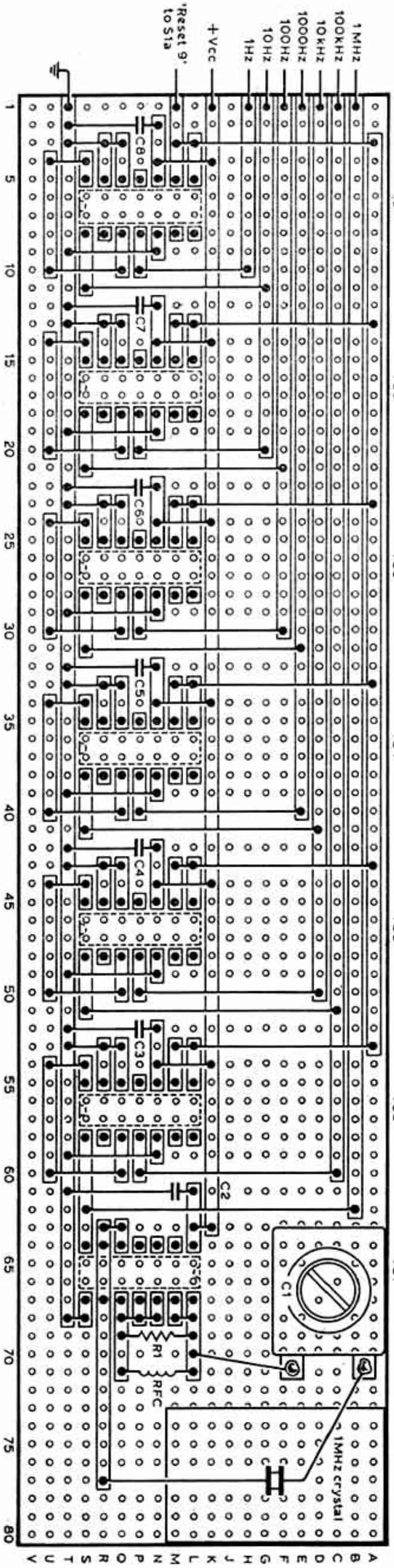


Fig 3. Veroboard layout of the clock board viewed from the copper side, the link wires and components being inserted into the reverse side

provided on the rear of the instrument giving access to the positive and negative low voltage supplies if required for ancillary equipment.

Construction

Two prototypes of the counter have been made, and while some readers may wish to adopt their own layout and techniques, constructional guidelines are included for those wishing to use them. The illustrations show clearly the relative positions of the components and the notes which follow may also prove useful.

The clock, control circuits and decade display boards are built on 0·1in matrix Veroboard. Details of the Veroboard panels are given in Figs 3, 4, 5 and 6. Each panel contains a minimum of discrete components and included on the clock panel is a Cathodeon 6V HC6U crystal oven currently available from *Radio Communication* advertisers. The diagrams of the Veroboard layout show the areas of copper which have been removed. Readers experienced in the use of Veroboard will appreciate that it is not essential to remove all unwanted copper provided a break is made in the appropriate places. However, it was felt that removal of all the unwanted copper produced a more tidy result. It should be mentioned here that the pulse measure facility was an added refinement and IC9 was built on a separate board. There is no reason why this circuit could not be incorporated on the main control board.

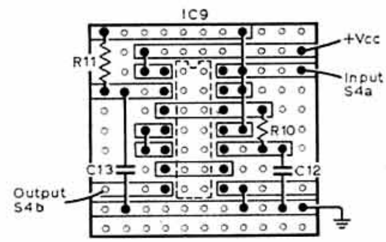


Fig 4. The pulse measure panel

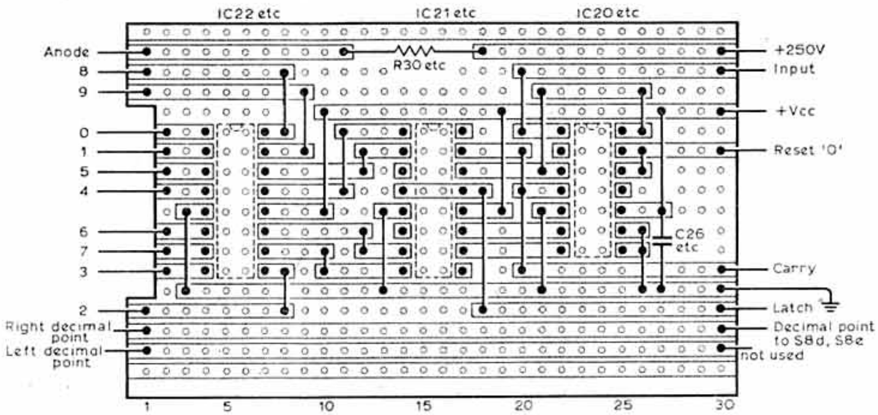
Components

A list of the components is shown in the table. A comment is necessary in regard to the seven-position push-button switch. A switch was obtained from J. Birkett of Lincoln but required minor modification for use in the counter. The locking mechanism on the "Reset 0" position should be removed, making the control a self-returning push button. Also, a set of the unused contacts on the "Reset O" position should be taken out and added to the "af/dc—rf" position, thereby making the latter a three-pole changeover switch.

Chassis and cabinet

The unit is assembled on a conventional four-sided chassis 9¼in by 6½in by 1in with aluminium base plate. The chassis is made from tinplate for ease of construction—it is made up of flat sheets soldered together. Brackets for fixing the base plate and Veroboard panels are also of tinplate soldered to the main chassis. The front and rear panels are 9⅝in by 3½in, 18swg aluminium, the tops of which are rounded to mate with a suitably shaped top cover, also of aluminium. After drilling, but prior to assembly of the components, a smart finish was obtained by painting the chassis and panels in

Fig 5. The display panel for cold cathode indicating tubes. Five of these are required



white gloss and the top cover in polychromatic violet in contrast. Instant lettering such as Panel Print (available from Doram Electronics Ltd) may be used for labelling the front panel and will provide a professional finish.

Assembly

It is recommended that assembly be carried out in the following sequence. The clock board should be built first and tested on a 5V positive supply. A temporary connection will be necessary between the "Reset 9" point and earth. An oscilloscope may be used to check the output from each stage or a receiver could be used to listen to the harmonics of the output. Accurate adjustment of the crystal frequency should be made with the trimmer C1 when the instrument is finally completed and the oven has been allowed to attain its normal working temperature. A standard frequency such as the BBC's 200kHz transmission or MSF may be used for this purpose.

Next the display boards should be made and tested individually using the 1Hz output from the clock board. Again a temporary connection will be necessary from the "Reset 0" point and earth. All five display boards may then be mounted together with the relevant interconnections and tested using any clock output. These boards may then be fitted to the chassis, and the control board, power supply and associated circuitry assembled.

Components list

R1	560Ω
R2	100kΩ
R3	120kΩ
R4	10kΩ
R5, 6, 8	47kΩ
R7	8·2kΩ
R9, 12, 26	1kΩ
R10, 11	180Ω
R13	82Ω
R14, 15, 16, 17	680Ω
R18, 19	270Ω
R20, 27, 29	1·5kΩ
R21	220Ω
R22	2·7kΩ
R23, 28	22kΩ
R24	33kΩ
R25	150Ω
R30, 31, 32, 33, 34	47kΩ, ½W
R35	22kΩ, 4W
R36	10Ω, 2W
RV1	10kΩ preset pot
RV2	4·7kΩ preset pot
RV3	50kΩ linear pot
C1	100pF compression trimmer
C2, 3, 4, 5, 6, 7, 8, 15, 16, 21, 26, 27, 28, 29, 30	10nF ceramic
C9	0·1μF polyester film
C10, 25	0·47μF 100V polyester film
C11, 14, 22	1,000pF feedthrough ceramic
C12, 13	1,000pF ceramic
C17, 19	47nF ceramic
C18, 20	100pF ceramic
C23	16μF 10V electrolytic
C24	160μF 6·4V electrolytic
C31, 34	10,000μF 12V electrolytic
C32	16μF 25V electrolytic
C33	8μF 350V electrolytic
IC1, 9, 14, 17, 19	SN7400
IC2, 3, 4, 5, 6, 7, 20, 23, 26, 29, 32	SN7490
IC8	SN7413
IC10	MC10116 Motorola
IC11	MC10131 Motorola
IC12	NE529K Signetics
IC13	SN74196
IC15, 16	SN7473
IC18	SN74121
IC21, 24, 27, 30, 33	SN7475
IC22, 25, 28, 31, 34	SN74141
IC35	MVR 5V Regulator (RS Components 305-377)
D1	Red indicator LED (RS Components 576-327)
D2	REC 63 (RS Components 261-491)
D3	1N4005 (RS Components 261-182)
D4	REC 70 (RS Components 261-328)
D5	BZX85 (6·2V) (RS Components 283-031)
TR1, 2, 3	2N706
S1, 2, 3, 4, 5, 6, 7	Seven-way push-button switch (see text)
S8	5-pole, 11-way rotary switch, "break" before "make"
S9	DPST miniature toggle switch
T1	4·5V + 4·5V, 20VA mains transformer (RS Components 207-122)
T2	250V 50mA, 6·3V 1·2A mains transformer (RS Components 196-117)

Cold cathode numerical indicator tubes
Heat sink for regulator (RS Components 401-497)
1,000kHz HC6U crystal
6V HC6U crystal oven (Cathodeon type MCO-2M)

RS Components items may be obtained from Doram Electronics Ltd, PO Box TR8, Wellington Road Industrial Estate, Leeds LS12 2UF.

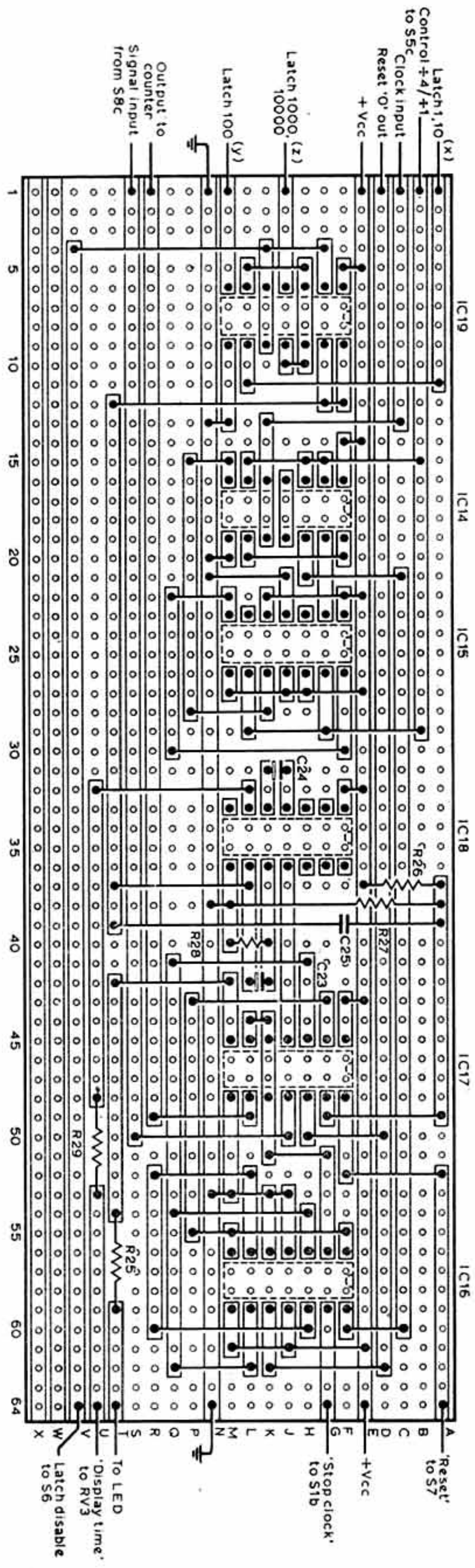


Fig 6. Veroboard layout of the main control panel. As in the other diagrams, the components and link wires are inserted into the other side of the panel

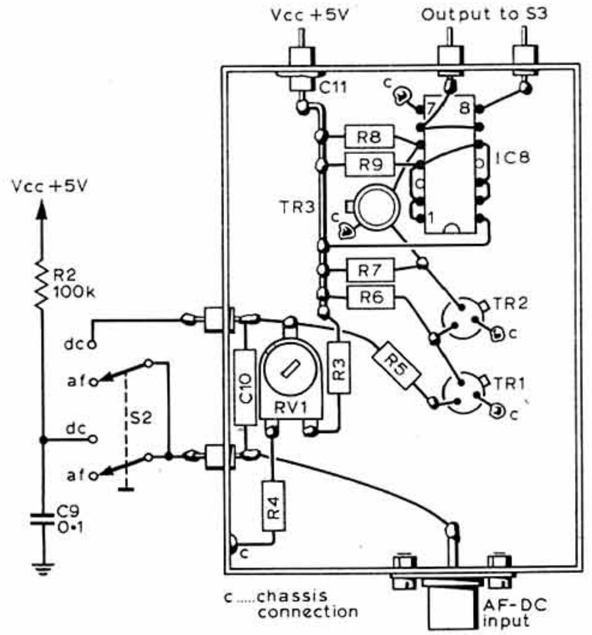


Fig 7. Layout diagram of the af/dc input circuit. TR1, TR2 and IC8 are shown viewed from the underside, while TR3 is mounted the other way round for ease of assembly

Input circuits

Each of the two input circuits is built into a small tinplate open box 2½in by 1¾in by ¾in soldered at the corners. The layout of the af/dc input components is shown in Fig 7. The supply voltage V_{cc} is taken via a feedthrough capacitor C11, while glass seals or nylon feedthroughs may be used for the outputs and connections to the af/dc switch S2. The side feedthroughs are positioned directly adjacent to S2 in order that the wiring to the switch may be as short as possible. The anti-bounce capacitor C9 and R2 are connected directly to the switch external to the af/dc input circuit sub-chassis. RV1 in the input circuit is provided to obtain optimum sensitivity and this will correspond to its maximum operating frequency.

Particular care should be exercised in the assembly of the rf input circuit, a suggested layout of which is shown in Fig 8. It will be desirable to build IC10 and IC11 as sub-assemblies before fitting them into the box. Readers may find it useful to refer to an article [1] in which the design and construction of the two input ICs was described. The potentiometer RV2 controls the bias on one input of the differential amplifier in IC12 and should be adjusted to give reliable operation.

Operation

The operation as a frequency counter is self-evident but it is felt that a few words of explanation are necessary in order to exploit the full potential of the instrument as a period timer.

With only the dc button depressed, a "make" condition on the af/dc input socket will start the instrument timing and a second "make" condition will stop it. The gate lamp will light on the first "make" and, unless the latch disable button is depressed, the timer will continue to read zero or

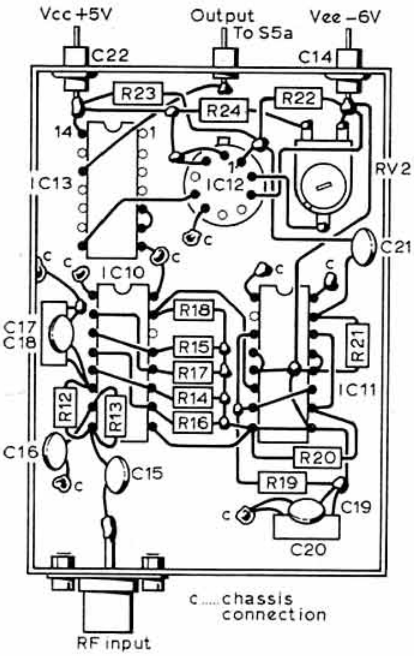


Fig 8. Layout diagram of the rf input circuit. The integrated circuits are shown viewed from the underside

the previous period measured. On the second "make" condition the gate lamp will go out and the timer will display the elapsed time.

The latch button may be used during a time measurement to provide the equivalent of a split-second hand on a stop watch.

When the trigger button is depressed, operation is the same as described above except that the timer is started or stopped with a "break" of a previously made contact.

The pulse measure button when operated allows the instrument to be started and stopped by consecutive "make" and "break" or "break" and "make" conditions.

With the stop clock button depressed the instrument will count the number of pulses fed to the input socket. For this facility the range switch should be in any frequency position and the latch disable button depressed.

Conclusion

Several instruments have been made to this design and their performance has fully met the design specification. The instrument described will provide a useful addition to any amateur station. Not only will it satisfy Post Office requirements in regard to frequency measurement, but will also enable time measurements to be made.

Reference

[1] "A 200MHz counter prescaler", D. J. Taylor, *Wireless World* January 1973, pp 27-8. □

WARC 1979

This phrase is heard whenever amateur service frequency allocations are under discussion. What is it? The initial letters stand for World Administrative Radio Conference which is to be held in the autumn of 1979 at Geneva under the auspices of the International Telecommunication Union. The decisions will be made by the delegates of the 147 member nations who will take part, and, in common with all UN organizations, the rule will be one country, one vote. The final terms of reference of the WARC have not yet been issued but it is likely that they will embrace all frequency allocations from 10kHz to 275GHz.

What is the amateur service doing about this event? The answer is, a lot; but at the moment it would be unwise to make public details of the planning. The Society has been advised by the Home Office that it will be fully involved in matters affecting the amateur service, and the Telecommunications Liaison Committee is fully briefed. Through the medium of the IARU Working Group and Region 1 IARU, the plans and thoughts of national societies are available. Make no mistake, it is only by the adoption of a world-wide plan, modified only to regional conditions, that the amateur service is going to survive in the form that we know it today.

Regions 1 and 3 (VK, ZL, JA etc) have already held their conferences and have agreed a plan. The Region 2 (N & S America) meeting is to be held in Miami commencing 11 April 1976 and will be followed by a meeting of the representatives of all three regions. What is to follow these discussions? The action is then for all national societies to put the plans to their administrations and secure their support at the WARC. Ultimately the only thing that counts is an "aye" vote at the conference. The difficulties lie not with the countries of W Europe, N America and the Commonwealth, who have traditionally supported the amateur service, but with many countries in Africa and Asia who see no value in amateur radio. Again it must be said that if it had not been for the support of the UK delegation at the 1971 Space Conference the amateur satellite service would not exist as we know it today. What is now needed is similar support from tens of countries round the world. This can only be achieved by continual effort from our representatives.

The national societies fully support the co-ordinating work of the IARU, and, in turn, are entitled to support from the radio amateurs who are the users of the frequencies.

The message is: **Support YOUR national society, the RSGB, and when on the air operate in a responsible manner.**

Dick Baldwin, W1RU, general manager of the ARRL, considers frequency allocation problems pointed out by G2BVN while Alfred Muller, DL1FL, looks on. The frequency chart formed part of the amateur radio stand at Telecom 75. *(Photo: DL1FL)*