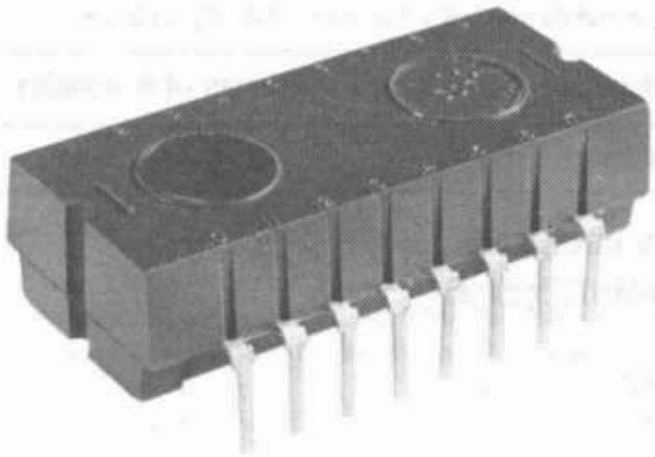
61 SERIES

61 SERIES THYRISTOR TRIGGER AND CONTROL MODULES

INTRODUCTORY NOTES



INTRODUCTION

This series comprises five modules. They may be used to produce most of the functions required to form simple and complex control systems in power engineering. The number of additional discrete components, usually required by such systems, has been kept to a minimum.

The main features of these modules are: -

1. Designed to drive the majority of thyristors and triacs.
2. Encapsulated for protection.
3. Working temperature range is -10 to +70°C (DOA61 is 0 to +70°C).
4. Suitable for use with wire-wrapping, soldering or printed-wiring boards.
5. Four easy mounting methods.

RANGE OF MODULES (for full details see individual data sheets)

Description	Function	Type number
Trigger transformer	Interface, giving two isolated outputs for use between thyristor or triac gates and control sections	TT61
Universal power amplifier	(a) Pulse generator for driving TT61 (b) D.C. driver (c) Other circuit functions	UPA61
Rectifier and synchroniser	Provides power supplies and synchronising signals	RSA61
Differential operational amplifier	For use in closed loop control systems	DOA61
Twin NOR	For logic functions	2NOR61

ACCESSORIES

(for full details see individual data sheets)

Description	Type number
Chassis for mounting a maximum of 21 printed-wiring boards	MC60 38240
Universal mounting chassis for mounting a maximum of 6 modules	UMC60
Mounting bar 1 metre long	MB60

CLIMATIC CATEGORY (IEC publication 68)

TT61, UPA61, RSA61, 2NOR61	10/070/56
DOA61	0/070/56

TEMPERATURE RANGE

Operating

TT61, UPA61, RSA61, 2NOR61	-10 to +70	°C
DOA61	0 to +70	°C

Storage

All modules	-40 to +85	°C

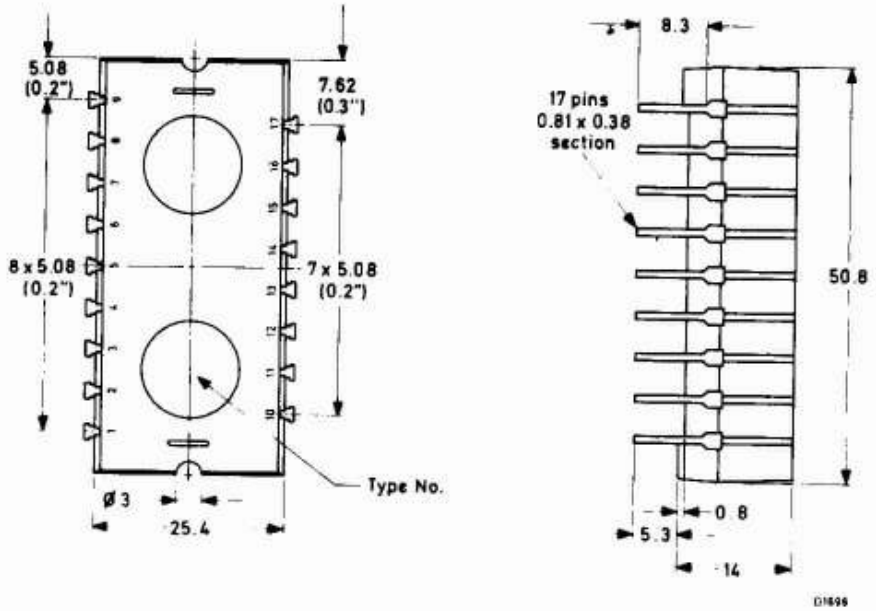
TERMINATIONS

The standard number of terminations on a module is 17. Each termination is a 0.81 × 0.38mm section pin which is suitable for mini-wrap (wires of up to 0.5mm diameter), modified mini-wrap (wires of up to 0.355mm diameter), soldering, or printed-wiring board use.

Termination numbers are moulded on both top and bottom of each module; all connections are accessible from both positions for test and servicing purposes.

DIMENSIONS (millimetres)

Modules



Accessories

See individual data sheets

WEIGHT	approx.	30	g

MOUNTING

1. By its terminations.

   Note: The terminations of each side of the modules are on a 5.08mm (0.2in) pitch but the two rows are staggered, and the modules must therefore be mounted on printed-wiring boards using the 2.54mm (0.1in) grid.

2. Universal mounting chassis UMC60 (see separate data sheet).

3. Mounting bar MB60 (see separate data sheet).

4. On a suitable flat surface using M2.5 screws or number 4 self-tapping screws.

TESTS

These modules are designed to meet the following IEC68 tests: -

1. Cold (functional), test A (except DOA61)	$-10^{o}C$
2. Dry heat (functional), test B (extended to 56 days)	$+70^{o}C$
3. Long term damp heat, test C	56 days
4. Vibration, test Fb	method A
5. Temperature cycling, test Na	-40 to $+85^{o}C$

The modules are also designed to meet the following: -

Shock test	3 blows at $490m/s^2$ (50g)

LOGIC DESIGN

The UPA61 and 2NOR61 may be used in logic systems; they may also be used in conjunction with the Mullard NORBIT 2 and 50 Series.

LOADING - drive units

In order to simplify system design, the input requirements and the output capability of the UPA61 and 2NOR61 are referred to in terms of DRIVE UNITS (d.u.).

A d.u. is an arbitrary unit of loading which takes into account the worst case condition for correct driving of the circuit and is referred to operation from a 24V (d.c.) ± 25% supply source. For example, a module circuit, having an output capability of 10d.u., may be used to drive a number of other circuit units with a total of input loading requirements not exceeding 10d.u. All units are designed to tolerate a capacitive loading of 200pF maximum at their outputs.

LOGIC LEVELS

The logic is considered to be positive logic, where the '1' level is more positive than the '0' level.

Logic '0' level is defined throughout the system as being a voltage between 0 and +0.3V.

A logic '1' level will be a positive voltage having a value determined by the loading, but which will approach the supply voltage level. This value must always be greater than 11.5V (when the power supply voltage is at a minimum) and the minimum value will rise with any increase in power supply voltage. Therefore, for a system operating from an 18V supply, the '1' level lies between 11.5 and 18V, whereas for a 30V supply it lies between 14.4 and 30V. Where the loading has been established in d.u., the requirements of voltage levels will automatically be met at all times.

D.C. NOISE IMMUNITY

'0' level immunity

A d.c. voltage of +1V with respect to the common (zero volt) line, applied to any one input (the other inputs floating), will not cause a change in output voltage.

'1' level immunity at 24V ± 25%

A variation of 2V below the minimum '1' input level, will not cause a change in output voltage.

'1' level immunity at 12V ± 5%

A variation of 0.25V below the minimum '1' input level, will not cause a change in output voltage.

ORDERING PROCEDURE

The modules and accessories should be ordered under their appropriate type numbers shown in the tables.

APPLICATIONS

The following are a few examples of typical applications: -

Static switch

D.C. driver

Simple phase control

Burst firing control

Fully controlled 3-phase a.c. controller

Parallel inverter drive

61 SERIES
RECTIFIER SYNCHRONISATION ASSEMBLY

RSA61

This data sheet should be read in conjunction with
61 SERIES THYRISTOR TRIGGER AND CONTROL MODULES - INTRODUCTORY NOTES

DESCRIPTION

This module has four basic functions: -

1. an unregulated +24V supply (with additional external electrolytic capacitor)
2. phase synchronising signals
3. stabilised -12V and +12V outputs (with additional external electrolytic capacitor)
4. additional components for various systems

ELECTRICAL DATA

Limiting values (these are absolute operating limits which must not be exceeded under any conditions).

Input supply r.m.s. voltage between pins 1 and 10			
for single rail output (see fig. 1)		16-22	V
for twin rail output (see fig. 2)		16-0-16 to 22-0-22	V
Supply source impedance		1 to 4	Ω
Output current			
at pin 7	max	8	mA
at pin 8	max	4	mA
Capacitance permissible at pin 16	max	1400	μF

Input data

This is the power supply, and the connections are shown in figures 1 and 2 on page 4.

Supply r.m.s. voltage			
for single rail output (fig. 1)		16 to 22	V
for twin rail output (fig. 2)		16-0-16 to 22-0-22	V
Supply current	max	375	mA

Output data

Outputs (referred to pin 9)				Capacitor details		
Nominal voltage (V)	Type of output	Current max (mA)	Pin number	Capacitance (μF) -20 +70% (see note 1)	Min working voltage (V)	Polarity and connecting pins (see figs. 1 and 2)
+24	Unregulated ± 25%	220	16	C1 = 800	40	+ve 16 -ve 9
+12 (see note 2)	Regulation = 2.6% max (open circuit voltage = 11 to 15V)	8	7			
-12	Regulation = 1.5% max (open circuit voltage = 11 to 14.25V)	4	8	C2 = 100	40	+ve 9 -ve 5

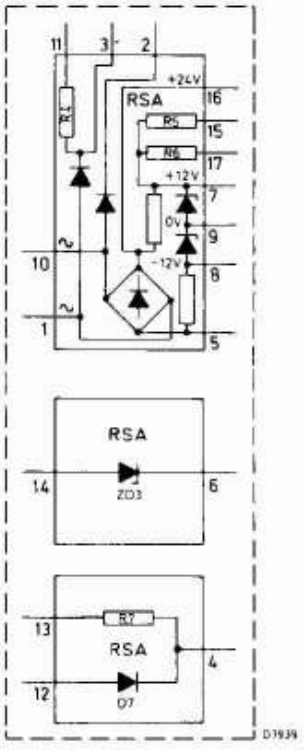
Notes:

1. In order to obtain a d.c. output, one or two capacitors are required (as shown in figures 1 and 2).
2. The +12V output is also brought out via two resistors (R5 and R6), for specific system requirements to pins 15 and 17

   R5 (pin 15) = 150kΩ ± 5%
   R6 (pin 17) = 100kΩ ± 5%

   Synchronising signals are fed via diodes to pins 2, 3 and 11. These signals are suitable for feeding into the UPA61.

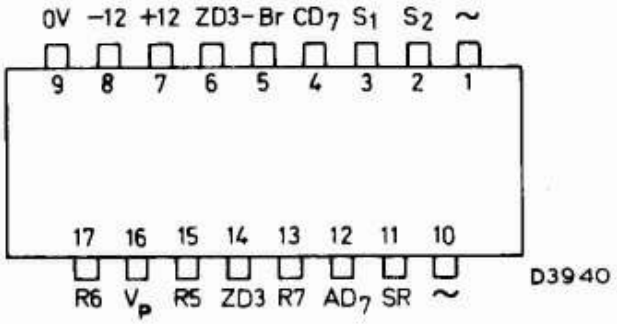
CIRCUIT DIAGRAM AND RECOMMENDED DRAWING SYMBOL



Ratings of extra internal components (see circuit diagram)

Component	Connection pins	Value
R7	4 and 13	2200Ω ± 10%, 30V max applied voltage
D7	12 and 4	V_R max = 30V, I_{FRM} max = 150mA
ZD3	14 and 6	V_Z nom (at I_z = 5mA) = 6.8V, 60mW dissipation max

TERMINAL CONNECTIONS



View from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	A.C. input (~)	10	A.C. input (~)
2	Synchronising output 2 (S_2)	11	Synchronising series resistor R4 (SR)
3	Synchronising output 1 (S_1)	12	Anode of diode D7 (AD_7)
4	Cathode of D7 and resistor R7 (CD_7)	13	Optional resistor R7 (R7)
5	Diode bridge -ve output (-Br)	14	Anode of voltage regulator diode (ZD3)
6	Cathode of voltage regulator diode (ZD3)	15	+12V, 150kΩ source (R5)
7	+12V output (+12)	16	+24V unregulated output (V_p)
8	-12V output (-12)	17	+12V, 100kΩ source (R6)
9	0V common (0V)		

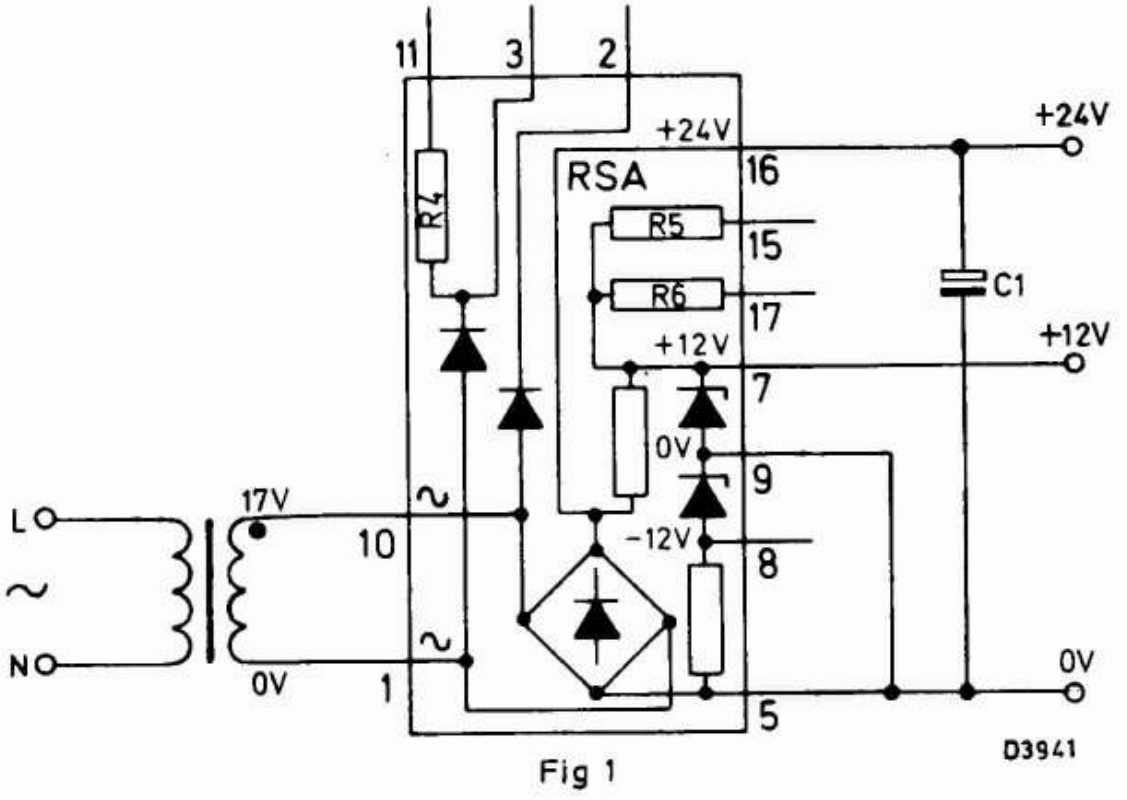


Fig 1

Connections for +12V and +24V (d. c.) outputs

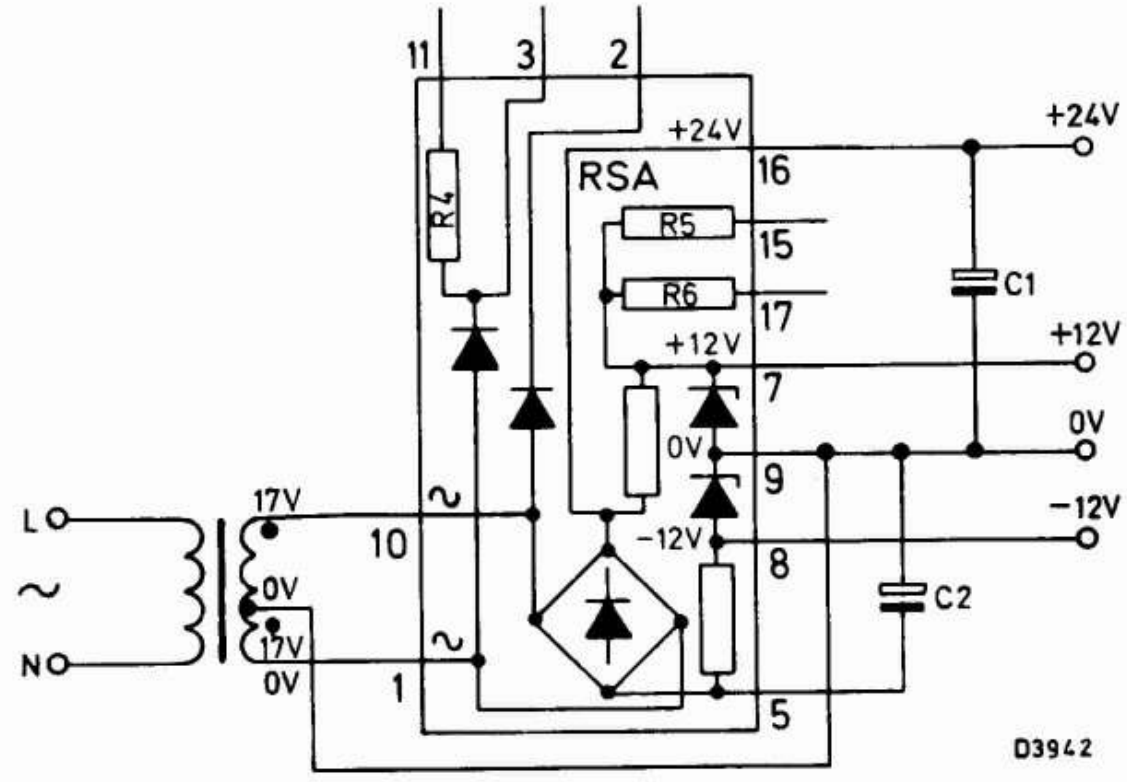


Fig 2

Connections for +12V, -12V, +24V (d. c.) outputs

61 SERIES
TRIGGER TRANSFORMER

TT61

TENTATIVE DATA

This data sheet should be read in conjunction with
61 SERIES THYRISTOR TRIGGER AND CONTROL MODULES - INTRODUCTORY NOTES

DESCRIPTION

The module functions as two identical isolating transformers within one encapsulation. It is particularly specified for use with the Mullard UPA61 module (connected as an oscillator) to interface thyristors and triacs with the control system. Thus both transformers may be current driven via the primary series resistors although the winding is terminated at both ends to allow other circuit configurations.

ELECTRICAL DATA

Limiting values (these are absolute operating limits which must not be exceeded under any conditions).

Primary switched voltage		30	V
Peak primary working current at pins 11, 12, or 15, 16, for duty cycle 1:3, and $T_{amb} = 25^{o}C$ (see note 1)		1.15	A
Max. d.c. continuous current at pins 10, 12 or 16, 17 and $T_{amb} = 25^{o}C$ (see note 2)		190	mA ←
ET product per transformer primary at pins 11, 12, or 15, 16		600	Vμs
Peak pulse power per transformer for duty cycle 1:3, and $T_{amb} = 25^{o}C$ (see note 3)		17	W
Test voltage (d.c.) between primary and secondary windings		4	kV
Continuous working voltage (r.m.s.) between primary and secondary windings		500	V
Operation from a UPA61			
Ambient temperature for continuous short circuit of one secondary		45	^{o}C
External series resistor connected to pins 11 or 15, pins 10 and 17 open circuit, duty cycle 1:2 (see note 4)	min	39 ±5%	Ω
Duty cycle with 39Ω external resistor		1:2	
80Ω internal resistor (see note 5)		1:3	

For notes see over

Notes:

1. Derate linearly at 7.8mA per deg C.
2. Derate linearly at 0.75mA per deg C. ←
3. Derate linearly at 110mW per deg C.
4. Separate UPA61s are required for each input when using external 39Ω resistors.
5. If a UPA61 fails to oscillate with the output transistor conducting, the primary series resistor may be damaged; circuit design must safeguard against this condition.

Transformer data

Turns ratio primary: secondary		3:1	
Inductance of primary (see note 1)	min	2.2	mH
Leakage inductance referred to primary with secondary short circuit (see note 1)	max	65	μH
Primary winding resistance at $T_{amb} = 25^{o}C$	max	3.62	Ω
Secondary winding resistance at $T_{amb} = 25^{o}C$	max	0.55	Ω

Input data

Frequency range (see note 2)	3 to 12.5	kHz
Primary switched voltage range	18 to 30	V

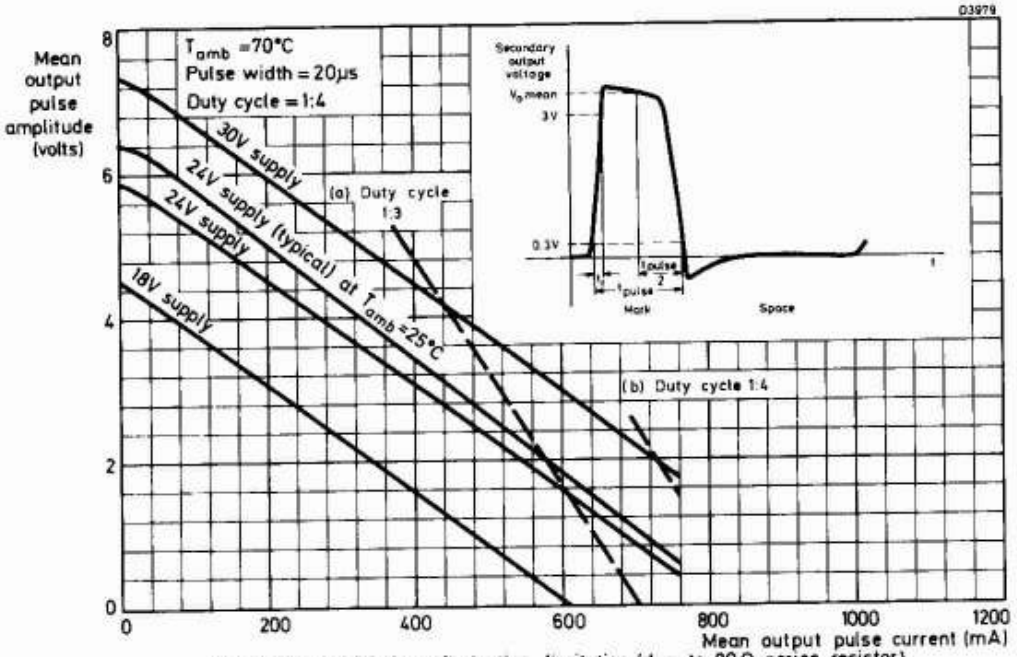
Notes:

1. Measured at 0.1V, 10kHz sinewave.
2. The minimum frequency has been specified with a view to core losses.

Output data

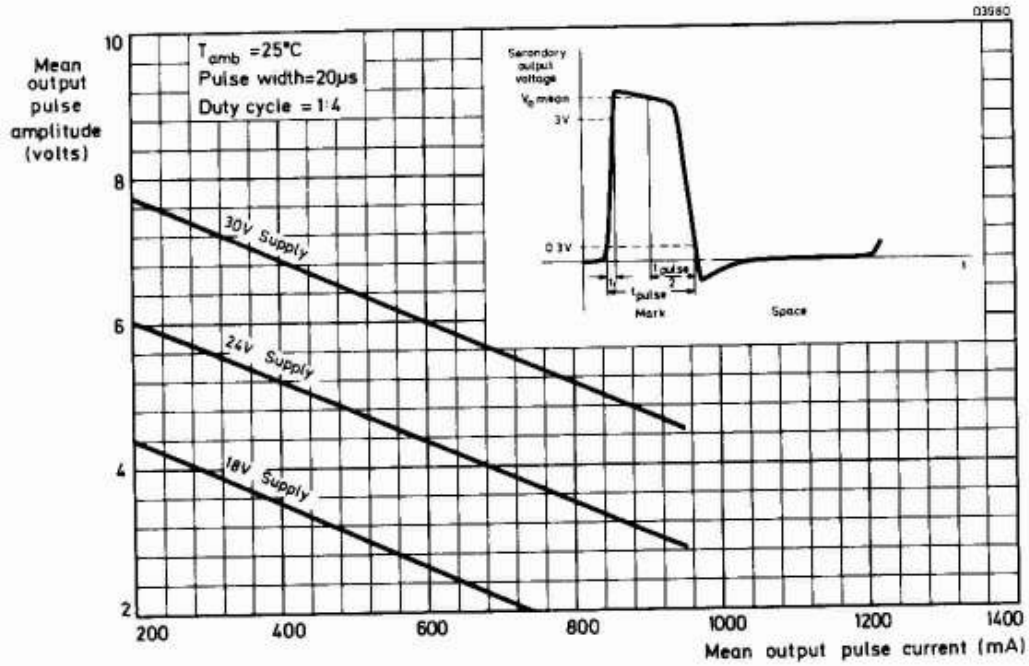
Output pulse response to a step input

Rise time, t_r, between 0.3 and 3V	typ	0.45	μs
	max	0.6	μs



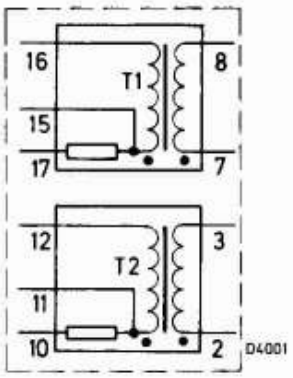
Curves (a) and (b) show dissipation limitation (due to 80Ω series resistor)

WORST CASE REGULATION CURVES
(INPUT VIA 80Ω INTERNAL RESISTOR)

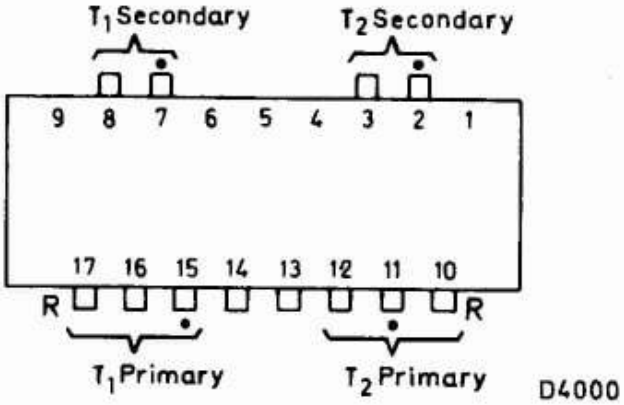


TYPICAL REGULATION CURVES
(INPUT VIA 39Ω RESISTORS CONNECTED TO PINS 11 AND 15
PINS 10 AND 17 OPEN CIRCUIT)

CIRCUIT DIAGRAM AND RECOMMENDED DRAWING SYMBOL



TERMINAL CONNECTIONS



View from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Not provided	10	T_2 primary series resistor
2	T_2 secondary start	11	T_2 primary start
3	T_2 secondary finish	12	T_2 primary finish
4	Not provided	13	Not connected
5	Not provided	14	Not connected
6	Not provided	15	T_1 primary start
7	T_1 secondary start	16	T_1 primary finish
8	T_1 secondary finish	17	T_1 primary series resistor
9	Not provided		

61 SERIES
UNIVERSAL POWER AMPLIFIER

UPA61

This data sheet should be read in conjunction with
61 SERIES THYRISTOR TRIGGER AND CONTROL MODULES - INTRODUCTORY NOTES

DESCRIPTION

This is a control module for use with the Mullard RSA61 and TT61, in power control systems, and comprising three main circuits: -

Emitter follower - transistor TR1
Trigger circuit - transistors TR2 and TR3
Switch power amplifier stage - transistor TR4

By making different interconnections between the above circuits, the following functions may be obtained: -

1. Trigger pulse generator
2. Variable frequency oscillator (by adding an external capacitor)
3. Voltage dependent delay
4. Current source
5. Emitter follower
6. Level detector
7. D.C. switched amplifier

ELECTRICAL DATA (over full temperature range, unless otherwise stated)

1. **Power supply**

Limiting value (this is an absolute operating limit, which must not be exceeded under any conditions).

Supply voltage (V_P)	+30	V

2. **Emitter follower (TR1)**

The circuit requirements are determined by the system application in which the module is used, and the component ratings.
Limiting values (these are absolute operating limits which must not be exceeded under any conditions).

Limit	V_{CEO}	I_C	I_{CM}	V_{EBO}	I_{EM}	P_{tot}	$V_{CE(sat)}$
maximum	30V	100mA	100mA	5V	100mA	400mW*	0.25V†

*for T_{amb} above 25°C derate at 4mW/degC

† at I_C = 10mA (I_C/I_B = 60) and T_{amb} = 85°C

3. **Trigger circuit (TR2, TR3)**

This is a regenerative bistable circuit, whose output is at one of two stable states, depending upon the d.c. input voltage. Inverted and non-inverted outputs are obtained from pins 4 and 3 respectively. The voltage at pin 3 will always be greater than +1 volt when TR3 is conducting and thus be unsuitable for driving grounded emitter circuits. Therefore, the output will normally be taken from pin 13, with the voltage regulator zener diode ZD1 in series.

3.1 **Limiting values** (these are absolute operating limits which must not be exceeded under any conditions).

	Limit	Pin 14	Pin 5 input resistor
Voltage	maximum	70V	30 V
	minimum	0V	0 V
Source impedance	maximum	200kΩ	250 kΩ
	minimum	0Ω	2.2kΩ

TR2		
Limit	V_{EBO}	I_B
maximum	6V	14mA

3.2 **Input data**

	V_P = +24V ± 25%	V_P = +12V ± 5%	
Tripping levels at pin 14			
Input voltage increasing	+11.5	+5.3	V
Input voltage decreasing	+1.8	+1.2	V
On and off tripping levels (hysteresis)	2.4 to 4.9	1.5 to 2.1	V
Input drive requirements at pin 4	2	2	d.u.

3.3 Output data

Supply voltage	Voltage range at pin 4	Used for driving into inputs		Via series voltage regulator diode
+24V ± 25%	7.5 to 15V	one 2NOR61	inputs 2, 4 only	BZY88/C8V2
		one 2NOR60 (NORBIT 2 range)	two inputs in parallel	BZY88/C8V2
+12V ± 5%	3 to 9V	one 2NOR61	inputs 2, 4 only	BZY88/C4V7

Notes:

(a) The trigger circuit output at pin 13 is designed to directly drive the base of TR4 at pin 6. When used in other circuit configurations, allowance must be made for leakage current through ZD1 when TR3 is conducting.

Leakage current through ZD1 (TR3 conducting) <50μA.

Max. load resistance between pins 13 and 9 for logic '0' level <6kΩ.

(b) The output at pin 4 may be used for logic purposes only in accordance with the table above and providing the UPA61 (pin 16) and the driven unit are energised from the same supply.

3.4 Supply current		V_P = +24V ± 25%	V_P = +12V ± 5%	
(TR2 conducting, pin 13 connected to pin 9)	max	16	5	mA

4. Power stage (TR4)

4.1 Limiting values (these are absolute operating limits which must not be exceeded under any conditions).

Limit	V_{CEO}	I_C	I_{CM}	V_{EBO}	P_{tot}	Current at pin 6
maximum	30V	2000mA	5000mA	5V	1.3W*	100mA

*for T_{amb} above 25°C, derate at 11mW/degC

4.2 Input data

Input at pin 6 to saturate TR4 (with R9 as collector load resistor)	>0.75	mA
TR4 base voltage for 'off' state	<0.3	V

ELECTRICAL DATA (contd.)

4.3 Output data

Load driver (load connected between pin 8 and 16)

	Directly driven	Driven via TR1
Load voltage	<30V	<30V
Load current	<330mA	<1A*
Load resistance (see note (a))	>90Ω	>30Ω (at 25°C)
Load inductance (with flywheel diode D2 in circuit) (see note (b))	<10H	<10H
Saturation voltage	<0.3V	<1.3V
Pin interconnections	6 to 13	8 to 11 6 to 10 1 to 12 to 13 to 17

*for T_{amb} above 25°C derate at 5mA/degC

Notes:

(a) When driving lamps, series and bleed resistors may be needed to limit the initial surge to prevent damage to TR4.

(b) When driving inductive loads, the cathode of diode D2 must be connected to the load supply to prevent damage to TR4.

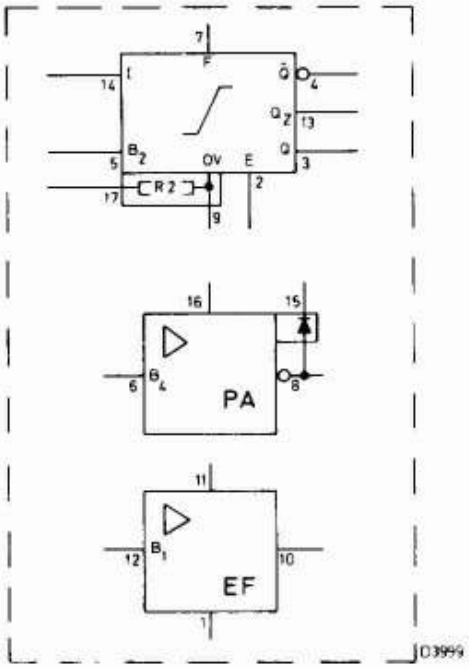
4.4 Logic output

Directly driven by the trigger circuit with pin 6 directly connected to pin 13.

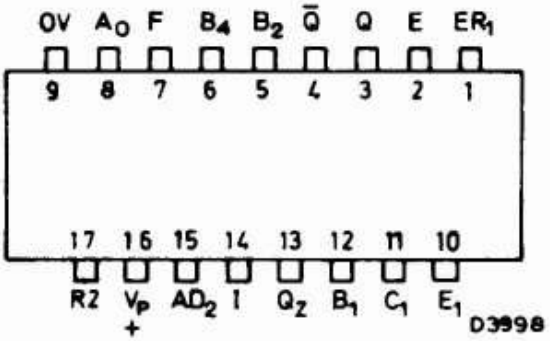
	V_P = +24V ± 25%	V_P = +12V ± 5%
Drive units	12 d.u.	Not applicable
Logic '0'	0 to +0.3V	0 to +0.3V
Logic '1'	(0.24V_P +7.2)V to V_P	(0.24V_P +5.5)V to V_P

	V_P = +18V	V_P = +11.4V
Typical available output current at logic '1' level	1.95mA	1.25mA

RECOMMENDED DRAWING SYMBOL



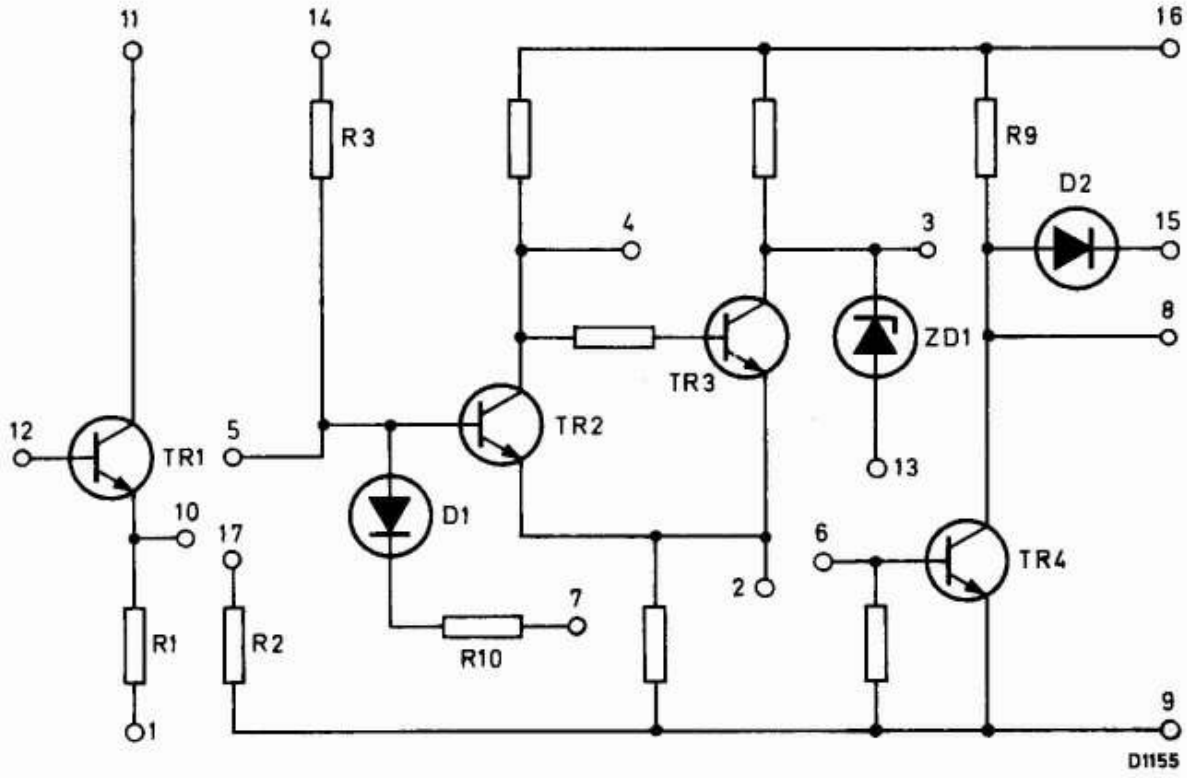
TERMINAL CONNECTIONS



View from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	TR1 emitter resistor (ER_1)	10	TR1 emitter (E_1)
2	Emitters-trigger circuit (E)	11	TR1 collector (C_1)
3	Trigger circuit normal output (Q)	12	TR1 base (B_1)
4	Trigger circuit complementary output ($\bar{Q}$)	13	Trigger circuit 0V level restored output (Q_Z)
5	Trigger circuit base input (B_2)	14	Trigger circuit input resistor (I)
6	Power stage base input (B4)	15	Power stage flywheel diode (AD_2)
7	Oscillator feedback terminal (F)	16	Positive supply voltage (V_P)
8	Power stage output (A_O)	17	Resistor R2)
9	0V common (0V)		

CIRCUIT DIAGRAM



	R1	R2	R3	R10
Resistance	22kΩ ± 10%	15kΩ ± 10%	47kΩ ± 10%	2.7kΩ ± 2%
Applied voltage	30V max.	30V max.	70V max.	-

2NOR61

This data should be read in conjunction with
61 SERIES THYRISTOR AND CONTROL MODULES - INTRODUCTORY NOTES

DESCRIPTION

The module comprises two identical dual input NOR units, with additional internal components to provide OR or INHIBIT functions as required. If any input of a 'NOR' is at the '1' level, then the output of that 'NOR' will be at the '0' level.

ELECTRICAL DATA

Power supply

Limiting value (this is an absolute operating limit, which must not be exceeded under any conditions).

Supply voltage (V_P)	+30	V

Characteristics

	V_P = +24V ± 25%	V_P = +12V ± 5%
Supply current (per NOR)	max 7.2	max 3.1 mA

NOR function

Limiting value (this is an absolute operating limit, which must not be exceeded under any conditions).

Input voltage (V_{in})	max +70	min -15	V

Input data

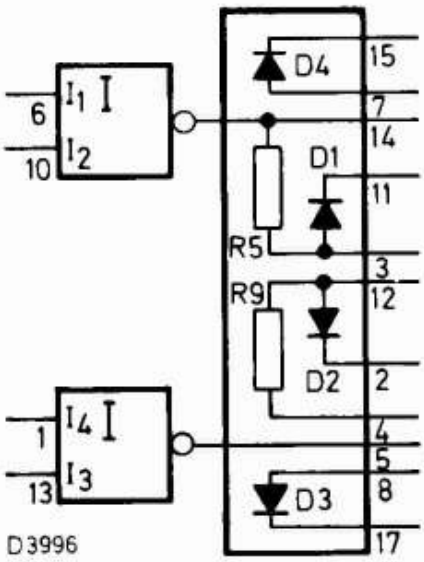
	V_P	
	+24V ± 25%	+12V ± 5%
Logic '0'	0 to +0.3V	0 to +0.3V
Logic '1'	(0.24V_P +7.2)V to +30V	(0.24V_P +5.5)V to +12.6V
Drive units (each input)	2d.u.	2d.u.

Typical input current	V_{in}	
	+11.5V	+8.25V
at inputs 1 and 3	0.21mA	0.15mA
at inputs 2 and 4	0.3 mA	0.21mA

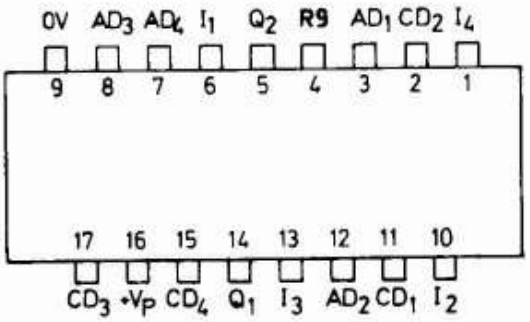
Output data

	V_P = +24V ± 25%	V_P = +12V ± 5%
Logic '0'	0 to +0.3V	0 to +0.3V
Logic '1'	(0.24V_P +7.2)V to V_P	(0.24V_P +5.5)V to V_P
Drive units	10d.u.	Not applicable
	V_P = +18V	V_P = +11.4V
Typical available output current at logic '1' level	1.5mA	0.73mA

RECOMMENDED DRAWING SYMBOL



TERMINAL CONNECTIONS

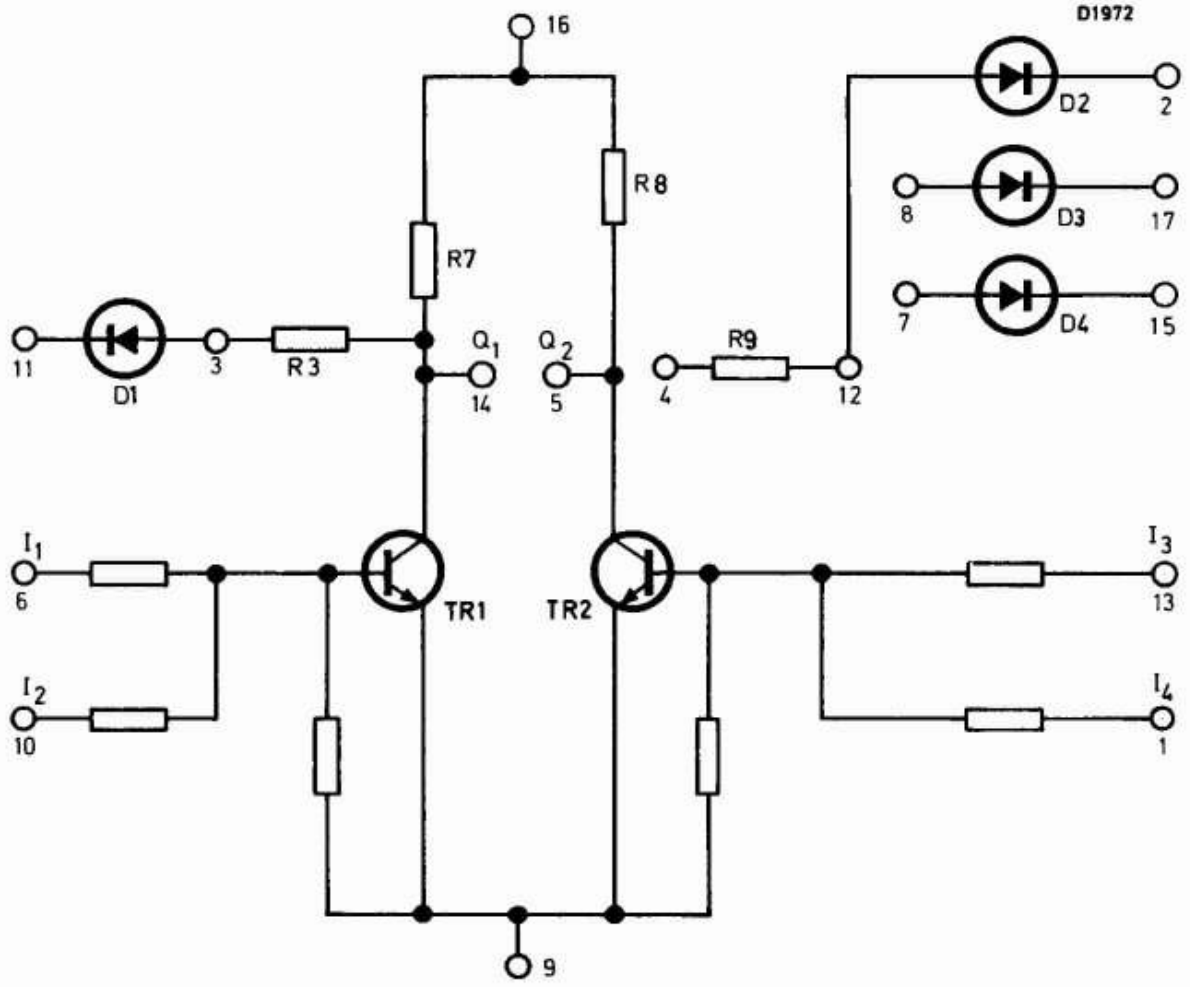


View from underside of module

Terminal number	Connected to	Terminal number	Connected to
1	Input 4 to NOR2 (I_4)	10	Input 2 to NOR1 (I_2)
2	Cathode diode D2 (CD_2)	11	Cathode diode D1 (CD_1)
3	Anode diode D1, resistor R3 (AD_1)	12	Resistor R9, anode diode D2 (AD_2)
4	Resistor R9 (R9)	13	Input 3 to NOR2 (I_3)
5	Output NOR2 (Q_2)	14	Output NOR1 (Q_1)
6	Input 1 to NOR1 (I_1)	15	Cathode diode D4 (CD_4)
7	Anode diode D4 (AD_4)	16	Positive supply input V_P (+V_P)
8	Anode diode D3 (AD_3)	17	Cathode diode D3 (CD_3)
9	Common supply (0V)		

2NOR61

CIRCUIT DIAGRAM

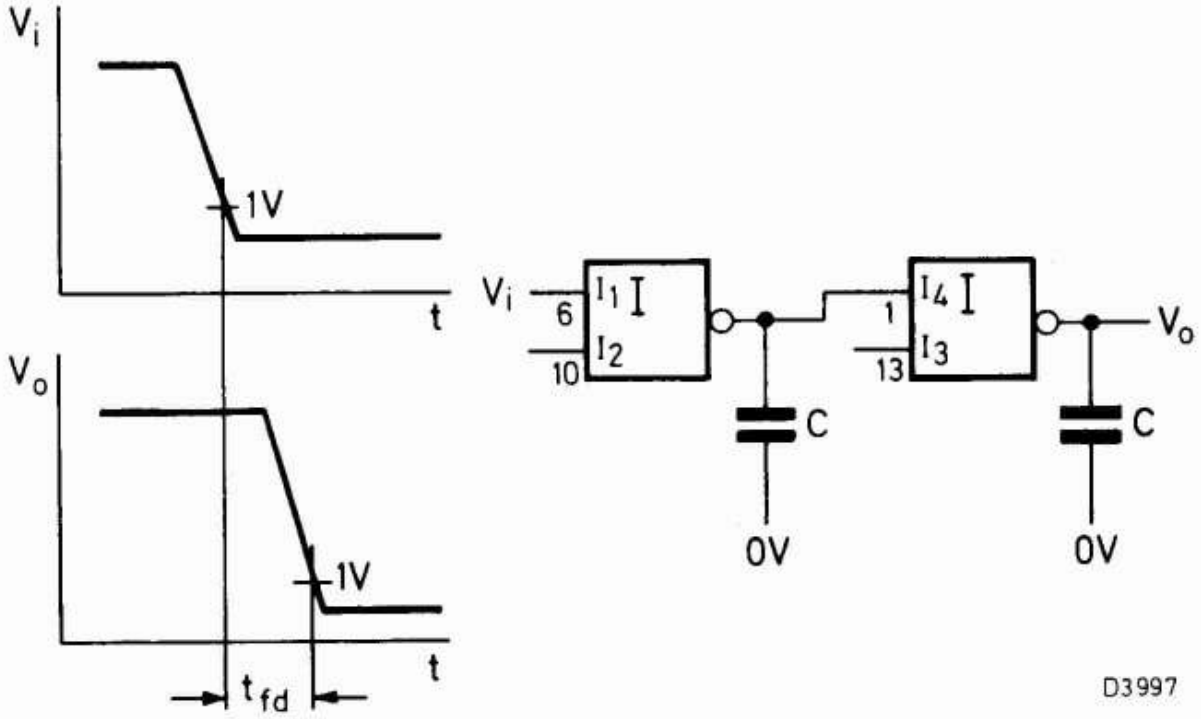


Ratings of extra internal components

Component	Connection pins	Value
D1	3 and 11	V_R max = 30V, I_{FRM} max = 20mA
D2	12 and 2	V_R max = 30V, I_{FRM} max = 20mA
D3	8 and 17	V_R max = 30V, I_{FRM} max = 20mA
D4	7 and 15	V_R max = 30V, I_{FRM} max = 20mA
R3	3 and 14	22kΩ ± 10%, 60V max applied voltage
R9	12 and 4	22kΩ ± 10%, 60V max applied voltage

PROPAGATION DELAY (t_{fd})

Over two stages	max	6μs



The delay time is defined as the time difference between the 1V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200pF (maximum permissible wiring capacitance).